MD01

(MEDALIST)

DISK CONTROLLER

TECHNICAL MANUAL

PRELIMINARY

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CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex Controller Product supplied shall be free from defects in material and workmanship.

During this period, if the customer experiences difficulties with an Emulex controller and is unable to resolve the problem via the phone with Emulex Technical Support, a Return Authorization will be issued. Following receipt of a Return Authorization, the customer is responsible for returning the product to Emulex, freight prepaid. Emulex, upon verification of warranty will, at its option, repair or replace the controller in question, and return to the customer freight prepaid.

CABLE WARRANTY: All Emulex provided cables, not included as part of a subsystem, are warranted for ninety (90) days from the time of shipment. Questionable cables should be returned to Emulex, freight prepaid, where they will be repaired or replaced by Emulex at its option and returned to the customer freight prepaid.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the Product, or use of the Product in such a manner for which it was not designed, or by causes external to the Product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace items covered in the above warranties. Purchaser shall provide for removal of the defective Product, shipping charges for return to Emulex and installation of its replacement.

RETURNED MATERIAL: Warranty claims must be received by Emulex within the applicable warranty period. A replaced product, or part thereof, shall become the property of Emulex and shall be returned to Emulex at Purchaser's expense. All returned material must be accompanied by a RETURN AUTHORIZATION number assigned by Emulex.

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Section 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The MD01 Disk Controller, called the Medalist, was designed by Emulex Corporation to interface Small Computer System Interface (SCSI) host adapters and controllers to one or two ST506 5.25-inch Winchester disk drives. (The SCSI bus can interface with up to eight host adapters and/or related microcontroller devices.) This manual is designed to help you install the MD01 Controller and to provide information about buffering, signal translation capabilities, and applications. The contents of the eight sections and one appendix are described briefly below.

Section 1	General Description: This section contains an overview of the MD01 Controller.
Section 2	MD01 Controller Specifications: This section contains specifications for the major components of the MD01 Controller.
Section 3	Installation: This section contains the information necessary to install the MD01 Controller in your system.
Section 4	Troubleshooting: This section describes diagnostic procedures that can be used to pinpoint problem areas on the MD01 Controller.
Section 5	Functional Description: This section describes the architecture and disk operations of the MD01 Controller.
Section 6	Interfaces: This section describes the SCSI bus and ST506 disk drive interfaces.
Section 7	SCSI Bus Protocol: This section describes the SCSI bus protocol, including signals, phases, and timing.
Section 8	MD01 SCSI Command Set: This section describes SCSI commands and their corresponding Command Descriptor Blocks, which are supported by the MD01 Controller.
Appendix A	General Error Conditions: This section describes general media-related and drive-related error conditions that can occur during MD01 Controller tape operations.

For reference convenience, Section 1 is divided into four subsections, as listed in the following table:

Subsection	Title
1.1	Introduction
1.2	Physical Description
1.3	Functional Overview
1.4	Compatibility

1.1.1 RELATED DOCUMENTS

This manual is designed to be used by system programmers who are writing operating system drivers and support utilities. Familiarity with the SCSI standard and the ST506 disk drive interface specification is assumed.

The Small Computer System Interface (SCSI) command set for the MD01 Controller is based on the ANSI X3T9.2/82-2 SCSI Specification, Revision 14 (01 May 1984). Copies of the ANSI SCSI Specification can be obtained from the following publisher:

American National Standard Task Group X3T9.2/82-2
Computer and Business Equipment Manufacturers Association
311 First Street, NW Suite 500
Washington, D.C. 20001

As the SCSI standard is currently changing, this ANSI specification is subject to change without notice. It is the intent of Emulex to maintain SCSI compatibility as the standard evolves.

The ST506 interface standard for 5.25-inch Winchester disk drives is described in standard #XXXXXXXXXX.

1.1.2 TECHNICAL MANUAL CONVENTIONS

To avoid possible confusion with other uses of the same words, throughout this manual we use the following conventions:

- All SCSI commands (such as **READ**, **MODE SELECT**, and **INQUIRY**) and diagnostic subcommands (such as **READ BAD SECTOR FILE** and **WRITE LONG**) are printed in uppercase boldface.
- All SCSI status and error messages (such as CHECK CONDITION and DRIVE NOT READY) are printed in uppercase.
- All SCSI bus phases and conditions (such as Arbitration Phase) and SCSI Command Descriptor Block names (such as Extended Sense Byte) are printed in initial caps.
- All SCSI command and message codes are given in their hexadecimal values.

1.2 PHYSICAL DESCRIPTION

The MD01 Controller, shown in Figure 1-1, is assembled on a single board approximately 14 centimeters by 20 centimeters (5.75 inches by 8 inches) and is installed directly on a mounting bracket located in the subsystem that contains an ST506 5.25-inch Winchester disk drive. The MD01 Controller contains two Emulex custom Very Large Scale Integration (VLSI) chips: a Buffer Controller and a Disk Formatter. It also contains an 8031 microprocessor chip, a 32K-byte Erasable Programmable Read Only Memory (EPROM), and a 16K-byte Random Access Memory (RAM) that provides 14K bytes of data buffering.

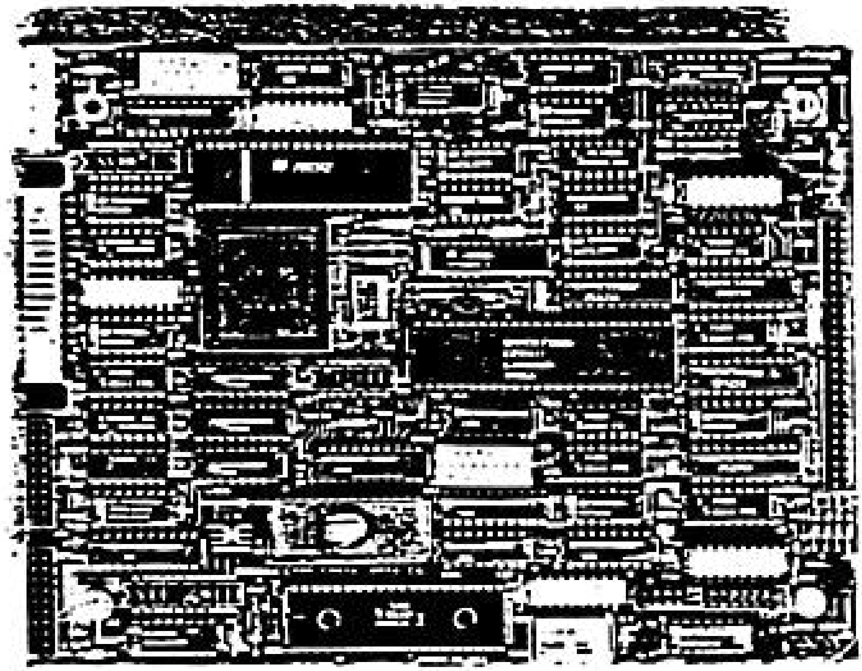


Figure 1-1. The MD01 (Medalist) Disk Controller

1.3 FUNCTIONAL OVERVIEW

In combination with an independent host adapter, the SCSI bus allows a wide variety of computers to interface with the MD01 Controller. Compatible computers include DEC systems that use the LSI-11 bus and the Unibus, IBM Personal Computer systems such as the IBM PC/XT, and Intel Multibus-based computers. Up to eight bus devices, in any combination of host systems and intelligent controllers, can be supported by the SCSI bus. The MD01 Controller, in combination with one or two ST506 5.25-inch Winchester disk drives, provides a low-cost, compact storage subsystem in a microcomputer environment.

The MD01 Controller's architecture and supported SCSI features make it an ideal building block for use by OEMs and system integrators. The MD01 Controller supports a powerful set of SCSI commands. By using those commands, an efficient multiple-Initiator configuration can be constructed with the support of the Disconnect function. (The Disconnect function allows the MD01 Controller, when it is performing a time-consuming task, to release the SCSI bus temporarily and reconnect at a later time when the task is complete.) The MD01 Controller may be considered a SCSI extended- bus device because all standard and extended SCSI commands are used.

Emulex currently offers two additional SCSI bus microcontrollers that can be used with SCSI bus subsystems: the Titleist and the Champion. The Titleist Tape Controller interfaces the SCSI bus to a streaming cartridge tape drive. The Champion Disk Controller interfaces Enhanced Small Disk Interface (ESDI) 5.25-inch disk drives to the SCSI bus.

In addition to basic stand-alone controller products, Emulex also offers complete SCSI bus disk and tape packaged subsystems for microcomputer applications.

Figure 1-2 shows a sample configuration of a SCSI system.

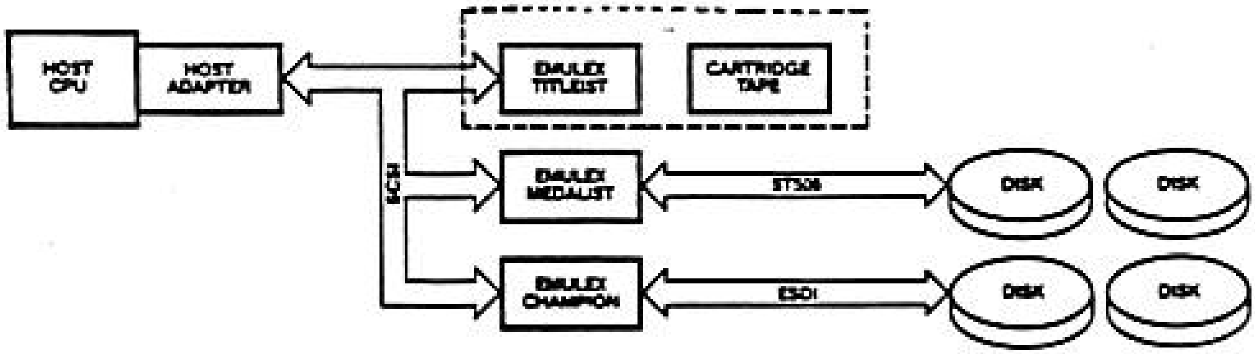


Figure 1-2. Sample SCSI Bus System Configuration

1.3.1 FEATURES

The MD01 Controller features are summarized below. More details on these features are given in subsequent sections.

- SCSI Implementation based on ANSI X3T9.2/82-2 Rev 14 (01 May 1984) Specification
- Support of standard 5.25-inch Winchester disk drives with ST506-compatible interfaces
- Powerful SCSI command set including:

  -Common Commands
  -Random Access Device Commands
  -COPY Command
  -Linked Command Support

- Support of disconnect/reconnect function
- Hard reset
- Buffered operation to optimize performances
- Extensive self-test and diagnostic facilities
- Compatible with Emulex's ESDI disk controller and streaming cartridge tape controllers

There are two Dual In-Line Package (DIP) switch packs on the MD01 Controller. Both switch SW1 and switch SW2 are eight-pole general control switches used for configuring various disk parameters. For configuration details, see Section 3 (Installation).

1.4 COMPATIBILITY

The following subsections describe compatibility of the MD01 Controller with ST506 disk drives and SCSI host adapter systems and related microcontrollers.

1.4.1 SCSI BUS HARDWARE COMPATIBILITY

A disk drive or tape drive that is connected to the SCSI bus and that follows the protocol outlined in the ANSI X3T9.2/82-2 SCSI Specification is compatible with the MD01 Controller/disk drive unit. A 50-pin male connector, reference designated J2, on the MD01 Controller plugs directly into the SCSI bus cable.

The MD01 Controller supports the SCSI bus single-ended bus option. The overall length of the cable that connects the SCSI host adapters and controllers in a daisy-chained manner can extend to 6 meters (20 feet). All SCSI signals in the cable are terminated at each end by terminating resistors of 220 ohms to +5 VDC, and 330 ohms to ground. Terminators are optionally installed, and depend on the physical profile of the SCSI bus (e.g., they would be installed if the MD01 Controller is used in an environment that includes an Emulex subsystem as the last device attached to the SCSI bus cable). The MD01 Controller complies with the FCC limits for a Class B computing device (see subsection 3.5).

1.4.2 SCSI BUS PROTOCOL AND COMMAND COMPATIBILITY

The MD01 Controller contains an on-board SCSI protocol controller that controls SCSI protocol and the SCSI bus. The MD01 Controller supports the SCSI arbitration and reselection capabilities, and data bus parity. The MD01 Controller supports all standard SCSI commands described in the ANSI X3T9.2/82-2 SCSI specification. For more information on commands supported by the MD01 Controller, see Section 8.

1.4.3 SCSI COMMAND SET

The hexadecimal codes for the SCSI commands supported by the MD01 Controller are shown in Table 1-1. Detailed command descriptions are given in Section 8.

Table 1-1. MD01 Controller SCSI Command Set

Group 0 Command	Hex Code	Group 0 Command	Hex Code
TEST DRIVE READY	00	REZERO UNIT	01
REQUEST SENSE	03	FORMAT UNIT	04
REASSIGN BLOCK	07	READ	08
WRITE	0A	SEEK	0B
INQUIRY	12	MODE SELECT	15
RESERVE UNIT	16	RELEASE UNIT	17
COPY	18	MODE SENSE	1A
RECEIVE DIAGNOSTIC	1C	SEND DIAGNOSTIC	1D
Group 1 Command	**Hex Code**	**Group 1 Command**	**Hex Code**
READ CAPACITY	25	SEEK (EXTENDED)	2B
READ (EXTENDED)	28	VERIFY	2F
SEARCH DATA EQUAL	31	WRITE (EXTENDED)	2A
SEARCH DATA HIGH	30	WRITE AND VERIFY	2E
SEARCH DATA LOW	32		

1.4.4 DEVIATIONS FROM SCSI STANDARD

When the MD01 Controller executes the **COPY** command (see subsection 8.3.1), it does not support copy operations for which neither the source or destination Logical Unit (LUN) is connected to an MD01 Controller; one of the peripheral devices involved in the copy operation must be connected to the MD01 Controller. However, the MD01 Controller does support the third-party reservation operation needed for the copy operation. The MD01 Controller supports block sizes of 256 and 512 bytes for external devices involved in the copy operation.

The MD01 Controller does not support the SCSI command queuing function.

The MD01 Controller does not check Reserved bits, fields, and bytes to ensure they are zero.

1.4.5 DISK DRIVE COMPATIBILITY

The MD01 Controller can be connected to any ST506 5.25-inch Winchester disk drive via a 34-pin control connector reference designated P1 on the MD01 Controller, and one or two 20-pin male data connectors reference designated J3 and J4 on the MD01 Controller. The MD01 Controller was designed specifically for use with ST506 5.25-inch Winchester disk drives.

2.1 OVERVIEW

This section contains the general, electrical, and physical specifications for the components on the MD01 Controller. A general description of each component is included under **FUNCTIONAL** in the General and Electrical Specifications table. For a detailed description of the MD01 Controller's function as a whole, see Section 5, Functional Description. The general, electrical, and physical specifications for the MD01 Controller are described in separate subsections as listed in the following table.

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications

2.2 GENERAL AND ELECTRICAL SPECIFICATIONS

Table 2-1 lists and describes the general and electrical specifications for the MD01 Controller.

Table 2-1. General and Electrical Specifications

Parameter	Description
FUNCTIONAL	
Design	High-speed microprocessor-based disk controller for integration of one or two ST506 5.25-inch Winchester disk drives to SCSI bus
SCSI Bus/Controller Interface	Standard SCSI bus interface (ANSI X3T9.2/82-2 specification), via a 50-pin male connector
Disk Drive Interface	ST506 interface for Winchester 5.25-inch disk drives, via a 34-pin drive control connector and a 20-pin data connector

continued on next page

Section 3
INSTALLATION

3.1 OVERVIEW

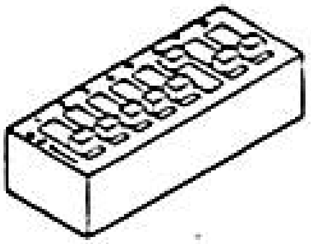
This section describes the step-by-step procedure for installing the MD01 Controller, including switch setting data and physical installation instructions. This installation procedure is divided into five subsections, as listed in the following table:

Subsection	Title
3.1	Overview
3.2	Inspection
3.3	MD01 Controller Setup
3.4	MD01 Controller Installation
3.5	FCC Compliance

If you are unfamiliar with the MD01 Controller installation procedure, we recommend that you read this Installation Section before beginning.

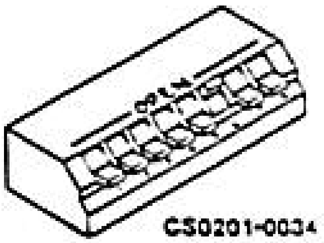
3.1.1 DIP SWITCH TYPES

DIP switches used in this product may be either of two types:



Slide Switch:

To place a slide switch in the ON position, slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, slide the switch in the direction marked OFF or OPEN.



Piano Switch:

To place a piano switch in the ON position, move the switch toward the ON or CLOSED position. To place a piano switch in the OFF position, move the switch toward the OFF or OPEN position.

Switch-setting tables in this manual use numeral one (1) to indicate the ON (closed) position and numeral zero (0) to indicate the OFF (open) position, except where noted.

3.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the MD01 Controller and verify that all components listed on the shipping invoice are present. Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on the shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

A visual inspection of the MD01 Controller is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components, or any other visual evidence of physical damage. Carefully examine all socketed components to ensure they are firmly and completely seated.

3.3 MD01 CONTROLLER SETUP

The switches in DIP switch packs SW1 and SW2 on the MD01 Controller allow configuration of various options available with the MD01 Controller. All switches on the MD01 Controller are set to a standard configuration before the MD01 Controller is shipped from the factory. DIP switch functions are listed and described in applicable tables in this section. Table 3-1 lists the functions and factory configurations of all switches on the MD01 Controller. This subsection provides an overview of the switch settings, as well as a description of the function of each switch.

Table 3-1. DIP Switch Settings, MD01 Controller

Switch	Factory Setting	Function	Section
SW1-1	OFF (0)	Encoded Drive Type (LSB)	3.3.1
SW1-2	OFF (0)	Encoded Drive Type	3.3.1
SW1-3	OFF (0)	Encoded Drive Type	3.3.1
SW1-4	OFF (0)	Encoded Drive Type	3.3.1
SW1-5	OFF (0)	Encoded Drive Type	3.3.1
SW1-6	OFF (0)	Encoded Drive Type (MSB)	3.3.1
SW1-7	OFF (0)	Soft Error Reporting Disable	3.3.2
SW1-8	OFF (0)	SCSI Bus Parity Check	3.3.3
SW2-1	OFF (0)	SCSI Bus Address (LSB)	3.3.4
SW2-2	OFF (0)	SCSI Bus Address	3.3.4
SW2-3	OFF (0)	SCSI Bus Address (MSB)	3.3.4
SW2-4	ON (1)	Must be set to ON	3.3.5
SW2-5	OFF (0)	Not Used	--
SW2-6	OFF (0)	Disable SCSI Bus Disconnect	3.3.6
SW2-7	ON (1)	Buffered Step Option	3.3.7
SW2-8	ON (1)	Drive Configuration Source	3.3.8

ON (1) = Closed
OFF (0) = Open

NOTE

These switch settings are subject to change.

Figure 3-1 shows the locations of the configuration switches, connectors, and jumpers referenced in the subsections below. The configuration switches should be set before the MD01 Controller and the disk drive are installed in a subsystem because the switches may not be accessible after the MD01 Controller/disk drive unit is installed.

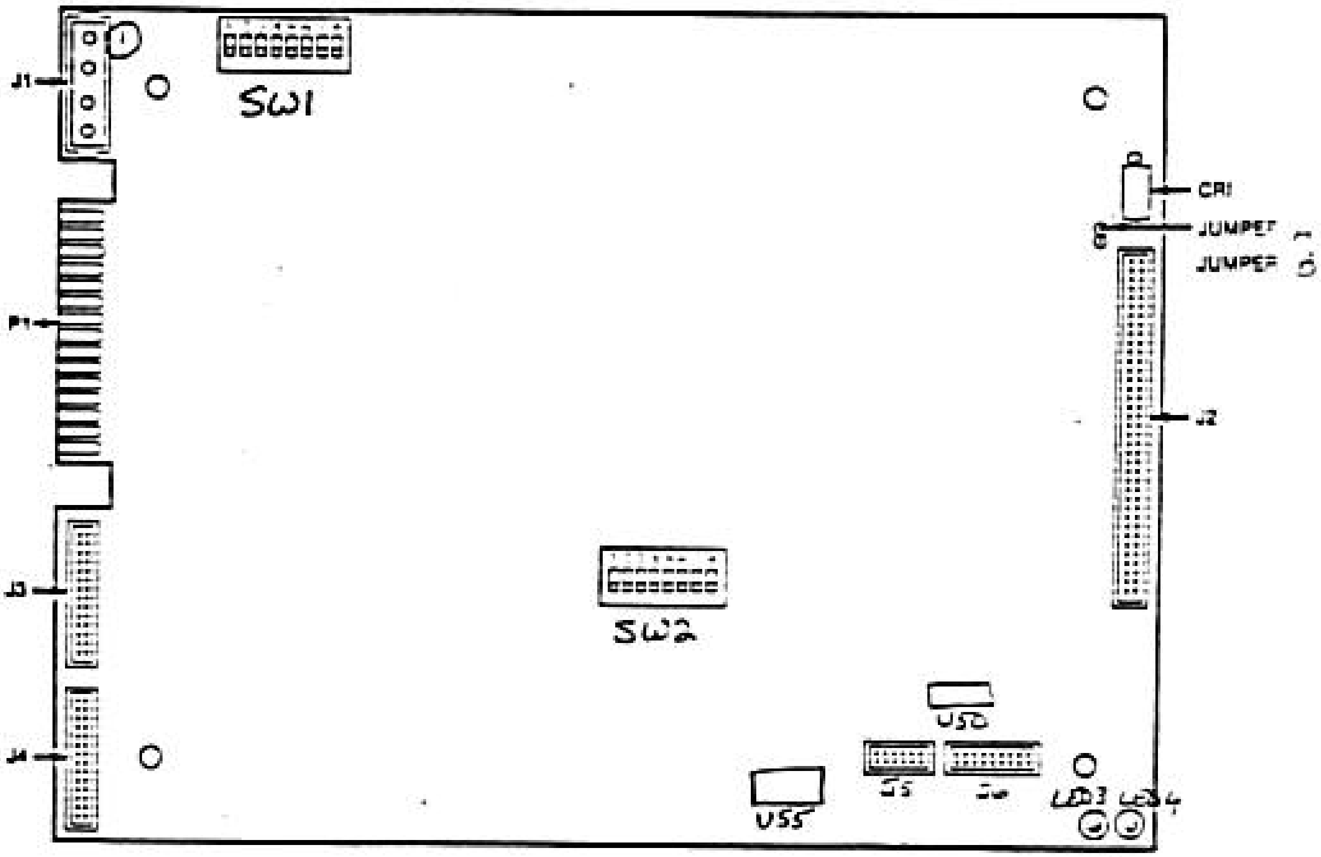


Figure 3-1. MD01 Controller Switch and Jumper Locations

3.3.1 ENCODED DRIVE TYPE (SW1-1 through SW1-6)

If switch SW2-8 is OFF (open), switches SW1-1 through SW1-6 are used to specify disk drive parameters. The switch settings specify a location in a table located in the firmware on the MD01 Controller. This table, called the Disk Drive Configuration Table, contains a list of all the disk drives currently supported by the MD01 Controller. Each disk drive entry in the table is associated with definitions of five parameters for that disk drive. The five parameters (and their corresponding mnemonic representations) are listed below.

- **Number of Sectors per Track (NST).** This parameter specifies the number of sectors per track. Note that since the sectors are numbered starting from sector zero, the last sector number on the track is equal to the total number of sectors per track less one.

- **Number of Heads (NH).** This parameter specifies the number of heads on the disk drive. Note that since the heads on the disk drive are numbered by starting from track zero, the last track address is equal to the total number of heads on the disk drive less one.

- **Number of Cylinders (NC).** This parameter specifies the number of cylinders on the disk drive. Note that since the cylinders on the disk drive are numbered starting from zero, the last cylinder address is equal to the total number of cylinders on the disk drive less one.

- **Write Precompensation Cylinder Number (WPC).** This parameter specifies the cylinder at which write precompensation is to begin. This value is vendor-dependent. Write precompensation is necessary for write operations to the inner cylinders (cylinders located near the center of the disk) because data in those cylinders is stored at a higher density than the density in the outer cylinders. When writing to inner cylinders, a magnetic effect (called peak shifting) occurs. This effect is caused by the tendency of closely spaced flux reversal domains to migrate physically away from each other into areas of lower density. In the time-precompensated format, flux reversals that would tend to be shifted late because of magnetic interference are written early, and those that would tend to be shifted early are written late.

- **Reduced Write Current Cylinder Number (RWC).** This parameter specifies the number of the cylinder at which the disk drive is to supply a different amount of current to the head during a write operation. The write current supplied to a selected head is not the same for all cylinder locations. More current is supplied for a write operation on an outer cylinder than is supplied for an write operation on an inner cylinder. If the write current is not reduced when writing on inner cylinders, flux saturation occurs which reduces frequency response and increases data interference (called crosstalk).

The disk drive entries (that specify those disk drive types supported by the MD01 Controller) contained in the Disk Drive Configuration Table are listed in Table 3-2. The parameters associated with each entry in the Disk Drive Configuration Table are listed in Table 3-3.

Table 3-2. Disk Drive Configuration Table Entries

Switch SW1-6 MSB	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1 LSB	Disk Drive Type	Config. Entry #
0	0	0	0	0	0	Atasi 3046 (256 byte sectors)	1
0	0	0	0	0	1	Atasi 3046 (512 byte sectors)	2
0	0	0	0	1	0	Rodime 208 (256 byte sectors)	3
0	0	0	0	1	1	Rodime 208 (512 byte sectors)	4
0	0	0	1	0	0	Fuji M224XAS (256 byte sectors)	5
0	0	0	1	0	1	Fuji M224XAS (512 byte sectors)	6
0	0	0	1	1	0	Maxtor Xt-1140 (256 byte sectors)	7
0	0	0	1	1	1	Maxtor Xt-1140 (512 byte sectors)	8
0	0	1	0	0	0	Wren II Model 94155-86 (256 byte sectors)	9
0	0	1	0	0	1	Wren II Model 94155-86 (512 byte sectors)	10

Config. Entry # = Disk Drive Configuration Table Entry Number

0 = OFF (OPEN)   1 = ON (CLOSED)

Table 3-3. Parameters for Entries in Disk Drive Configuration Table

Configuration Table Entry Number	NST	NH	NC	WPC	RWC
1	32	7	645	320	320
2	16	7	645	320	320
3	32	8	640	640	*
4	16	8	640	640	*
5	32	11	754	0	*
6	16	11	754	0	*
7	32	15	920	none	*
8	16	15	920	none	*
9	32	9	917	none	*
10	16	9	917	none	*

NST = Number of Sectors per Track
NH = Number of Heads
NC = Number of Cylinders
WPC = Write Precompensation Cylinder Number
RWC = Reduced Write Current Cylinder Number

* For these disk drives, the Reduced Write Current signal and the Head Select signal are on the same line. This signal is used as the most significant bit of the Head Select and therefore is not used for Reduced Write Current.

3.3.2 SOFT ERROR REPORTING DISABLE (SW1-7)

Switch SW1-7 indicates if the MD01 does or does not report soft errors that occur during MD01 disk operations. Setting switch SW1-7 to ON (closed) causes the MD01 to not report soft errors. Setting switch SW1-7 to OFF (open) causes the MD01 to report soft errors. Normally, switch SW1-7 is set to OFF, as described in the following table:

Switch	OFF	ON	Factory
SW1-7	Soft errors are reported	Soft errors are not reported	OFF

NOTE

If you are using the IB01 Host Adapter (designed by Emulex for use with an IBM PC system) with Revision A or B firmware, SW1-7 on the MD01 Controller must be set to ON.

3.3.3 SCSI BUS PARITY CHECK (SW1-8)

The MD01 Controller always generates odd parity on the SCSI bus. However, the MD01 Controller must be configured to check odd parity on the SCSI bus. Switch SW1-8 indicates if the MD01 Controller does or does not check odd parity on the SCSI bus. Setting switch SW1-8 to ON (closed) causes the MD01 Controller to check odd parity on the SCSI bus. Setting switch SW1-8 to OFF (open) causes the MD01 Controller not to check odd parity on the SCSI bus. The use of parity is a system option. All SCSI bus devices must generate and detect parity, or all SCSI bus devices must not generate and detect parity. Parity is not valid during the Arbitration Phase (see subsection 7.3.1). Normally, switch SW1-8 is set to OFF, as described in the following table:

Switch	OFF	ON	Factory
SW1-8	Parity is not not checked	Parity is checked	OFF

3.3.4 SCSI DEVICE ADDRESS SELECTION (SW2-1 through SW2-3)

Switches SW2-1, SW2-2, and SW2-3 are used to select any one of eight possible SCSI bus addresses for the MD01 Controller. The selected address establishes the SCSI bus identity for the MD01 Controller in the system. An Initiator must specify this address to select the MD01 Controller as a Target device. Switch settings for the eight possible MD01 Controller Device Address identities are listed in Table 3-4. Verify the same SCSI Device Address is not assigned to two separate host adapters or controllers.

Table 3-4. SCSI Device Address Selection Switches

SW2-3 (MSB)	Switch SW2-2	SW2-1 (LSB)	SCSI Device Address
0	0	0	00
0	0	1	01
0	1	0	02
0	1	1	03
1	0	0	04
1	0	1	05
1	1	0	06
1	1	1	07
0 = OFF (OPEN) 1 = ON (CLOSED)			

3.3.5 PROPRIETARY FUNCTION (SW2-4)

Switch SW2-4 is used for a proprietary function and must remain set to ON as shown in the following table:

Switch	OFF	ON	Factory
SW2-4	Not used	Proprietary function	ON

3.3.6 DISABLE SCSI BUS DISCONNECT (SW2-6)

The setting on SW2-6 indicates if the SCSI disconnect function is disabled. If it is, the MD01 Controller does not support the SCSI bus disconnect function. This function allows the MD01 Controller to temporarily release a SCSI bus connection to a host so that the MD01 Controller can complete a time-consuming task. The MD01 Controller can then reconnect to the host once the task is complete.

Setting switch SW2-6 to ON (closed) indicates the SCSI disconnect function is disabled. Setting switch SW2-6 to OFF (open) indicates the SCSI disconnect function is enabled. Normally, switch SW2-6 is set to OFF, as shown in the following table:

Switch	OFF	ON	Factory
SW2-6	Disconnect function enabled	Disconnect function disabled	OFF

NOTE

When switch SW2-6 is ON, the MD01 Controller ignores bit 06 of the SCSI IDENTIFY message (see subsection 7.3.3.4).

3.3.7 BUFFERED STEP OPTION (SW2-7)

The setting on switch SW2-7 determines whether the disk drive step operation (involving the time intervals in which Step signal pulses occur) is or is not to be buffered. If the disk drive supports a buffered step operation, the MD01 Controller performs an optimum buffered seek operation with 11 microsecond step pulses. During nonbuffered seek operations, the MD01 Controller waits for a seek operation to complete before performing another one. Setting switch SW2-7 to ON (closed) causes the step operation to be buffered. Setting switch SW2-7 to OFF (open) causes the step operation to be not buffered. Normally, switch SW2-7 is set to ON, as listed in the following table:

Switch	OFF	ON	Factory
SW2-7	Nonbuffered	Buffered	ON

3.3.8 DRIVE CONFIGURATION SOURCE (SW2-8)

Switch SW2-8 determines which set of disk drive configuration parameters the MD01 Controller will use. The MD01 obtains configuration parameters either from the settings on switches SW1-1 through SW1-6 or from sector 0 on the disk drive (which stores host-specified parameters).

NOTE

> If the MD01 is installed in an environment that includes an Emulex DEC host adapter (or any SCSI host adapter that supports the **MODE SELECT** command), SW2-8 should be set to ON.

When switch SW2-8 is OFF (open), the MD01 uses the parameters associated with the disk drive type specified by switches SW1-1 through SW1-6 (see subsection 3.3.1).

When switch SW2-8 is ON (closed), the MD01 Controller uses host-specified configuration parameters, which are stored on sector 0 of the disk drive. If the MD01 Controller is connected to an unformatted disk drive, it cannot obtain disk configuration parameters from sector 0. In this situation, to specify disk parameters, the host must issue a **MODE SELECT** command (see subsection 8.3.5). The host must then issue the **FORMAT UNIT** command (see subsection 8.4.2) to cause the MD01 Controller to write these parameters onto sector 0.

NOTE

> If you set switch SW2-8 to indicate that the Encoded Drive Type switches (SW1-1 through SW1-6) are valid, ensure that you have set those switches correctly to reflect the type of disk drive installed.

Normally, switch SW2-8 is set to ON, as shown in the following table:

Switch	OFF	ON	Factory
SW2-8	Switches SW1-1 through SW1-6	Configuration parameters on sector 0 of formatted disk drive	ON

NOTE

> If two different types of disk drives which do not have the same parameters (such as sector size and number of sectors/track) are connected to the same MD01 Controller, SW2-8 must be set to ON so that the MD01 can use the parameters on sector 0 of each drive.

3.3.9 SCSI BUS TERMINATION POWER OPTION

The SCSI Termination option is used if the MD01 Controller is resident in an Emulex subsystem. It allows the MD01 Controller to supply +5 VDC power to the subsystem's external terminators via pin 26 of the SCSI bus. The SCSI Termination option is not required if the MD01 Controller is resident in an Emulex subsystem that contains an internal terminator power board.

If the SCSI Termination option is required, install a #1N5817 diode at reference designator CR1 on the MD01 Controller printed circuit board assembly (PCBA). Also connect a wire-wrap jumper between jumper posts J and K on the MD01 Controller (see Figure 3-1) to supply +5 VDC for the SCSI bus termination.

CAUTION

> If diode leads are reversed so that the anode of the diode is in the wrong hole, the system does not function properly. (The cathode end of the diode has a band of color to identify polarity; the anode end of the diode is plain.)

3.3.10 SCSI BUS TERMINATION

The MD01 Controller can be configured to terminate the SCSI bus by inserting one 220/330 ohm resistor pack in each of the two sockets located at U50 and U55 on the MD01 Controller (see Figure 3-1). The resistor packs are available in the Emulex SCSI terminators kit, P/N MD0113002. A SCSI system configuration should only contain two devices that terminate the SCSI bus. Usually these devices are a host adapter and one peripheral device controller (such as the MD01 Controller).

3.4 MD01 SCSI CONTROLLER INSTALLATION

To install the MD01 Controller in the disk drive chassis, see Figures 3-2 through 3-4 and use the following procedure:

1. Configure the MD01 Controller. This action involves setting the switches on switch packs SW1 and SW2 before installing the MD01 Controller on the mounting bracket in the subsystem that contains the disk drive(s). All switches have been set at the factory; however, you may need to reset certain switches to satisfy your specific needs.

2. Place the disk drive subsystem on a flat surface.

3. Place the MD01 Controller (component side up) on top of the mounting bracket. Align the four screw holes on the MD01 Controller with the four screw holes on the mounting bracket (see Figure 3-2). Secure the MD01 Controller in place with four 4-40 x 0.25-inch screws.

4. Connect the control cable from the disk drive to 34-pin connector P1 on the MD01 Controller (see Figure 3-3).

5. Connect the data cable from the disk drive to 20-pin connector J3 and/or J4 on the MD01 Controller (see Figure 3-3).

6. Connect the cable from the power supply to power connector J1 on the MD01 Controller (see Figure 3-3).

7. Connect the SCSI bus cable to SCSI bus connector J2 on the MD01 Controller (see Figure 3-4).

NOTE

Note that Figure 3-4 shows a SCSI flat-ribbon cable that is used to internally connect the MD01 Controller with a SCSI host adapter. If the MD01 Controller and SCSI host adapter reside in different cabinets, you must use a shielded SCSI cable to connect them to maintain FCC compliance (see subsection 3.5). For more information on shielded cable requirements, see subsection 6.2.1.2.

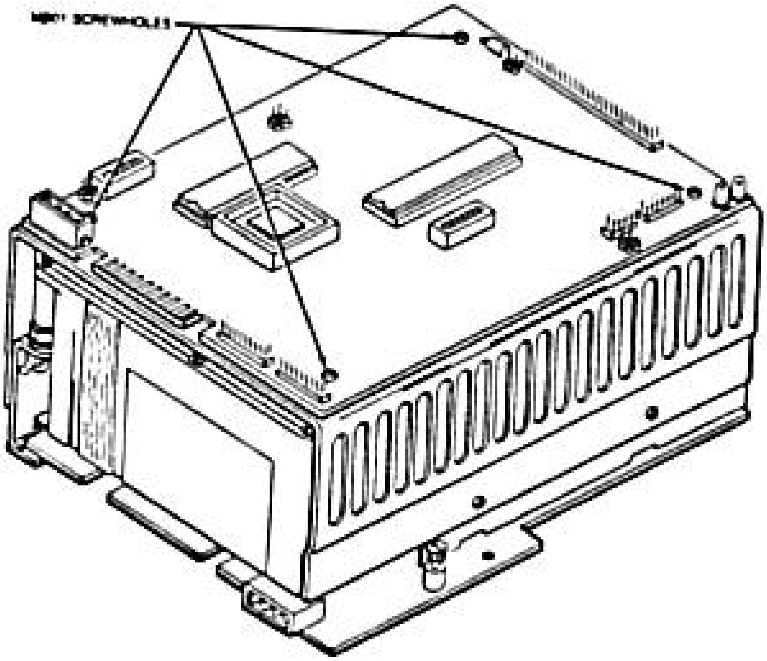


Figure 3-2. Installing MD01 Controller on Mounting Bracket

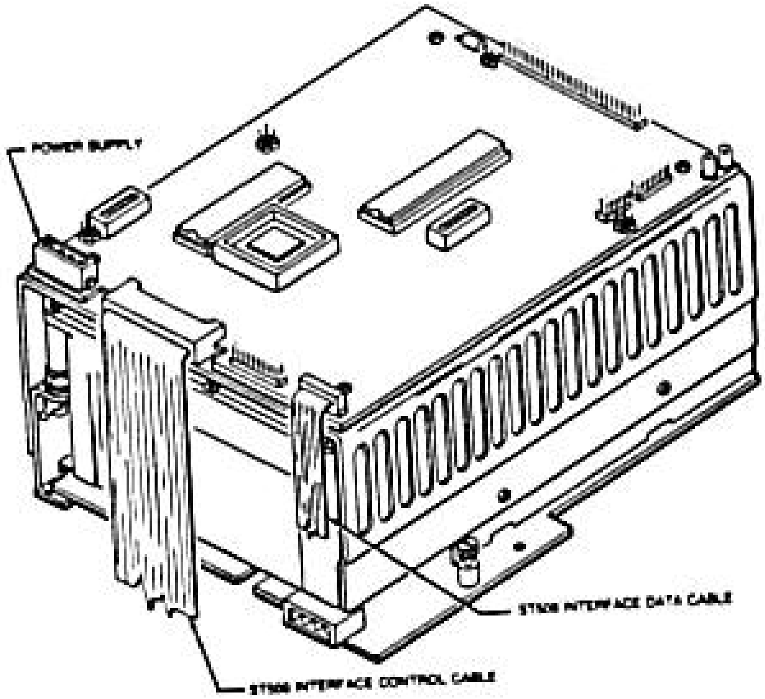


Figure 3-3. Connecting Disk Drive Data and Control Cables to MD01 Controller

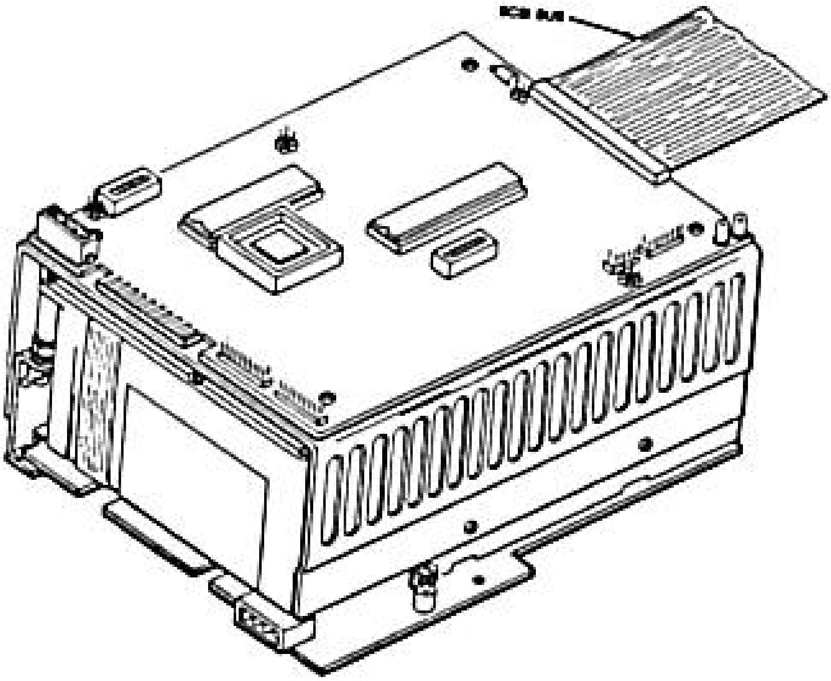


Figure 3-4. Connecting SCSI bus to MD01 Controller

3.5 FCC COMPLIANCE

The Federal Communications Commission (FCC) has established technical standards regarding radiation of electromagnetic interference (EMI) emitted by computing devices. The MD01 Controller has been type tested and found to comply with the EMI emission limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. However, there is no guarantee that interference will not occur in a particular installation.

The MD01 Controller was tested for FCC compliance in a compliant subsystem that was properly shielded (enclosed so that no electromagnetic radiation escapes). The subsystem was connected to other SCSI port devices via a shielded SCSI bus cable. Emulex offers shielded cables, compatible with the MD01 Controller, that are available in various lengths. For information on SCSI bus cable and connector requirements, see subsection 6.2.1.

Since the MD01 Controller equipment generates and uses radio frequency energy, if it is not installed and used in strict accordance with Emulex's instructions, it may cause EMI with radio and television reception. It is the responsibility of the user to properly install the MD01 Controller and ST506 disk drive in a compliant subsystem. MD01 Controller installation instructions are described in subsection 3.4. Emulex is not responsible for any radio or TV interference caused by unauthorized modifications to the MD01 Controller.

If the MD01 Controller does cause interference with radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the compliant subsystem (that contains the MD01 Controller) with respect to the receiver.
- Move the compliant subsystem away from the receiver.
- Plug the compliant subsystem into a different outlet so that the subsystem and receiver are on different branch circuits.
- Verify the mounting screws and grounding wires on the compliant subsystem are tightly secured.

If necessary, you should consult the dealer or an experienced radio/television technician for additional suggestions. You may find helpful a booklet prepared by the FCC, How to Identify and Resolve Radio-TV Interference Problems. It is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

Section 4
TROUBLESHOOTING

4.1 OVERVIEW

This section describes the diagnostic features with which the MD01 Controller is equipped. MD01 Controller diagnostic modes include power-up (and reset) self-test and on-line host-initiated diagnostic facilities. The principal function of these tests is to determine MD01 Controller functional integrity and to distinguish between failures of the MD01 Controller and the disk drive. This section is divided into four subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Power-Up Self-Test
4.3	Online Diagnostic Commands
4.4	MD01 Controller LEDs

4.1.1 SERVICE

The components of your Emulex MD01 Controller have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

If one of the diagnostic procedures described in this section indicates a component is not working properly, the MD01 Controller must be returned to the factory, or to an Emulex authorized repair center, for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex. whether the product is or is not under warranty. you must contact Emulex's Technical Support for instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN AN MD01 CONTROLLER TO EMULEX WITHOUT AUTHORIZATION. An MD01 Controller returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States. Alaska. and Hawaii contact:

Emulex Customer Support
3545 Harbor Boulevard
Costa Mesa. CA 92626
(714) 662-5600 TWX 910-595-2521

Outside the United States, contact the distributor from whom the MD01 Controller was initially purchased.

After you have contacted Emulex and received an RMA number, package the MD01 Controller (preferably by using the original packing material) and send the MD01 Controller **POSTAGE PAID** to the address given you by the Emulex representative. The sender should also insure the package.

4.2 SELF-TEST PROCEDURES

The MD01 Controller performs a self-test procedure when it operates in either of two modes: the normal mode or the burn-in mode. These two modes and their corresponding self-test procedures are described in the following subsections.

4.2.1 NORMAL MODE

The MD01 Controller operates in the normal mode when it performs typical disk controller functions such as a disk format operation or a read operation. When the MD01 Controller is operating in the normal mode and power-up or reset conditions occur, it performs a self-test procedure to determine if its interface circuits, memory, and on-board microprocessor are operative. The self-test procedure consists of several individual tests that exercise separate components of the MD01 Controller. These tests are performed sequentially; the success of one test enables the next test to be executed. If an individual test fails, the MD01 Controller self-test procedure stops at the location of the failure.

Before the self-test procedure begins, a Power-up Reset Clear code is output to the two on-board LEDs to indicate that the MD01 Controller is ready to perform a self-test. If the MD01 Controller self-test procedure succeeds, a Self-Test Pass code is output to the on-board LEDs. The LED locations on the MD01 Controller are shown in Figure 4-1, and LED Test Code descriptions are listed in Table 4-1.

Table 4-1. LED Test Code Descriptions

LED 4	LED 3	Test Description
0	0	Power-up Reset Clear
1	1	Power-Up Self-Test Pass Code
0 = OFF (not lit) 1 = ON (lit)		

If the MD01 Controller is operative, LED 3 (see subsection 4 4) blinks. If the MD01 Controller fails its self-test procedure, LED 3 does not blink.

After the self-test procedure is successfully completed, the MD01 Controller continues with the initialization routine. If the SCSI interface circuits and the 8031 microprocessor are functioning, the MD01 Controller enters the on-line mode and is available to the Initiator. At this time, the Power-Up Self-Test Pass Code (see Table 4-1) is displayed by LED 3 and LED 4. Failures in the Disk Formatter and/or disk drive result in a CHECK CONDITION status code in response to the completed **TEST UNIT READY** command (see subsection 8.3.15) or in response to a completed data transfer command (such as **READ** or **WRITE**). Further analysis of these failures can be made by using the **SEND DIAGNOSTIC** command (see subsection 8.3.14).

NOTE

> If the MD01 Controller self-test procedure is initiated on-line (via the **SEND DIAGNOSTIC** command, see subsection 8.3.14), the host-supplied device parameter definitions are lost. If the default parameters had been overridden previously, the host must resubmit the parameters to the MD01 Controller by using the **MODE SELECT** command (see subsection 8.3.4).

4.2.2 BURN-IN MODE

During the burn-in mode, the MD01 Controller self-test procedure is repeated continuously until a failure is detected. The MD01 Controller contains an eight-bit burn-in connector used to report self-test failures when the MD01 Controller is operating in the burn-in mode. The burn-in connector consists of four pin assignments on the test connector, reference designator J6 on the MD01 Controller (see Figure 3-1), and four pin assignments on the User's Panel connector, reference designator J5 on the MD01 Controller (see Figure 3-1). The burn-in connector pin assignments are shown below:

	Bit							
	07	06	05	04	03	02	01	00
Connector	J6-9	J6-8	J6-7	J6-12	J5-4	J5-6	J5-7	J5-9

As each individual test is performed during the MD01 Controller burn-in mode, a test code is output to the burn-in connector to indicate which component on the MD01 Controller is currently being tested. If an individual test fails, the corresponding test code is output. The individual tests in the self-test procedure and their corresponding codes are listed in Table 4-2. (The codes are listed in their hexadecimal notations.)

To establish the MD01 Controller burn-in mode. ground pin J6-5 Once the burn-in mode has been established. to cause the MD01 Controller to perform its self-test procedure continuously. ground pin J5-8 and reset the MD01 Controller.

Table 4-2. MD01 Controller Test Code Descriptions

Test Code * (hexadecimal)	Test Description
00	Power-up Start Code
01	Buffer Controller Reset Status Test
02	Disk Formatter Reset Status Test
04	SCSI Reset Latch Test
40	8031 Microprocessor Self-Test
41	ROM Checksum Test
42	Buffer Controller LSI Register Test
43	External RAM Data Test
44	External RAM Parity Test
45	Buffer Controller LSI Parity Detection Test
46	Buffer Controller LSI Parity Interrupt Test
81	Disk Formatter LSI Register Test
83	SCSI Controller LSI Self-Diagnostic Test
84	SCSI Controller LSI Interrupt Test
85	SCSI Controller LSI Register Test

* Asserted bits are low true

4.3 ONLINE DIAGNOSTIC COMMANDS

The MD01 Controller supports a set of online diagnostic subcommands. which are used to further delineate peripheral or MD01 Controller failures. These diagnostic subcommands are specified by the **SEND DIAGNOSTIC** command and executed by the **RECEIVE DIAGNOSTIC** command. The diagnostic subcommands are listed in Table 4-3 and described in subsection 8.3.14.

NOTE

The host may detect the diagnostic subcommand execution has been completed if the MD01 Controller responds to other commands after it has been reset. If a failure occurs. the MD01 Controller halts. The host can issue a SCSI bus reset instruction to cause a retry of the diagnostic procedures. Execution of the self-test procedure automatically resets the MD01 Controller.

Table 4-3. MD01 Controller Diagnostic Subcommands

Diagnostic Subcommand	Description
PERFORM DRIVE DIAGNOSTICS	Causes MD01 Controller to perform write and verify operations on each surface of the diagnostic cylinder.
READ BAD SECTOR FILE	Causes MD01 Controller to transfer the contents of the Bad Sector File to the Initiator.
READ DISK PARTITIONS	Causes MD01 Controller to transfer the physical addresses related to the logical partitions on the specified disk drive to the Initiator.
READ LONG	Causes MD01 Controller to perform a read operation of one data block and its 6 bytes of ECC. starting at the specified block address.
WRITE LONG	Causes MD01 Controller to perform a write operation of one data block and its 6 bytes of ECC. starting at the specified block address.

4.4 MD01 CONTROLLER LEDS

The locations of the two MD01 Controller on-board LEDs are shown in Figure 4-1.

LED 3 is mounted on the MD01 Controller and indicates the status of the MD01 Controller. LED 3 blinks on and off when the MD01 Controller is operating properly. LED 3 remains either illuminated or extinguished if the MD01 Controller malfunctions or has encountered a fatal hardware condition. If this last situation occurs. the MD01 Controller must be reset to recover from the fatal hardware condition.

LED 4 is mounted on the MD01 Controller and is currently not used.

MD01 Controller LEDs

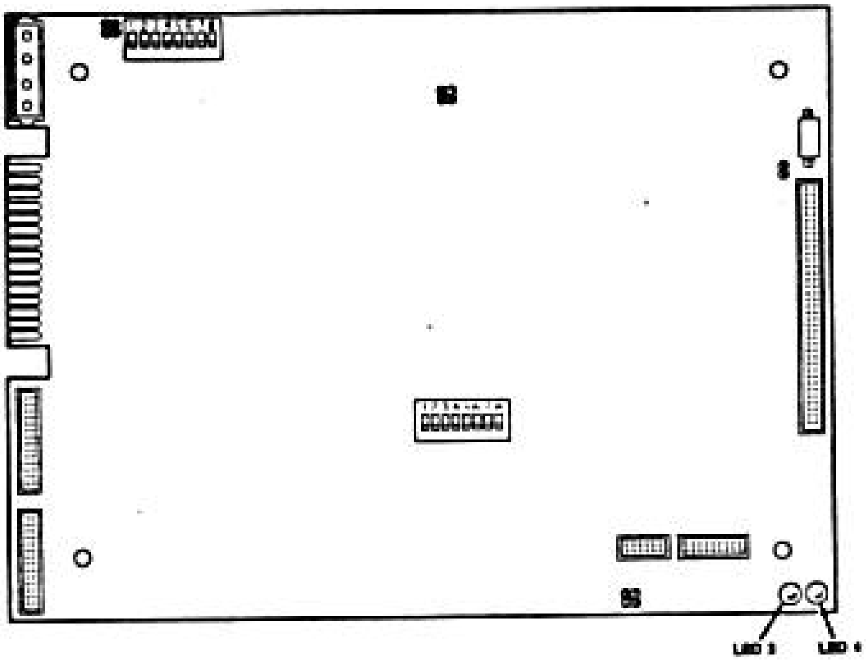


Figure 4-1. Location of LEDs on the MD01 Controller

5.1 OVERVIEW

This section describes MD01 Controller architecture and disk operation. For reference convenience, this section is divided into three subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	MD01 Controller Architecture
5.3	Disk Operations

.2 MD01 CONTROLLER ARCHITECTURE

Figure 5-1 is a block diagram that shows the major functional elements of the MD01 Controller. The MD01 Controller is organized around the 8031 microprocessor, and the Disk Formatter and Buffer Controller custom VLSI chips designed by Emulex.

Two buses are used in the MD01 Controller: the data bus and the microprocessor bus.

The data bus is connected directly to the Disk Formatter, buffer memory, and Buffer Controller. The Buffer Controller is connected directly to the buffer memory and the microprocessor bus. Therefore, the data bus and Buffer Controller provide a data path between the registers in the Disk Formatter, the buffer memory, and the 8031 microprocessor.

The microprocessor bus provides a path for transmission of control and status information. This information may be passed between the 8031 microprocessor, the EPROM, the Buffer Controller, and the Disk Interface.

5.2.1 8031 MICROPROCESSOR

The 8031 microprocessor (with the Disk Formatter) controls all disk drive operations. These operations include drive control, head positioning, and reading drive status. The Disk Formatter controls formatting of the data that is written to, and read from, the disk drive. The 8031 microprocessor generates Read and Write commands that are executed by the Disk Formatter. All Read and Write commands involve operations only on a single data block (256 or 512 bytes).

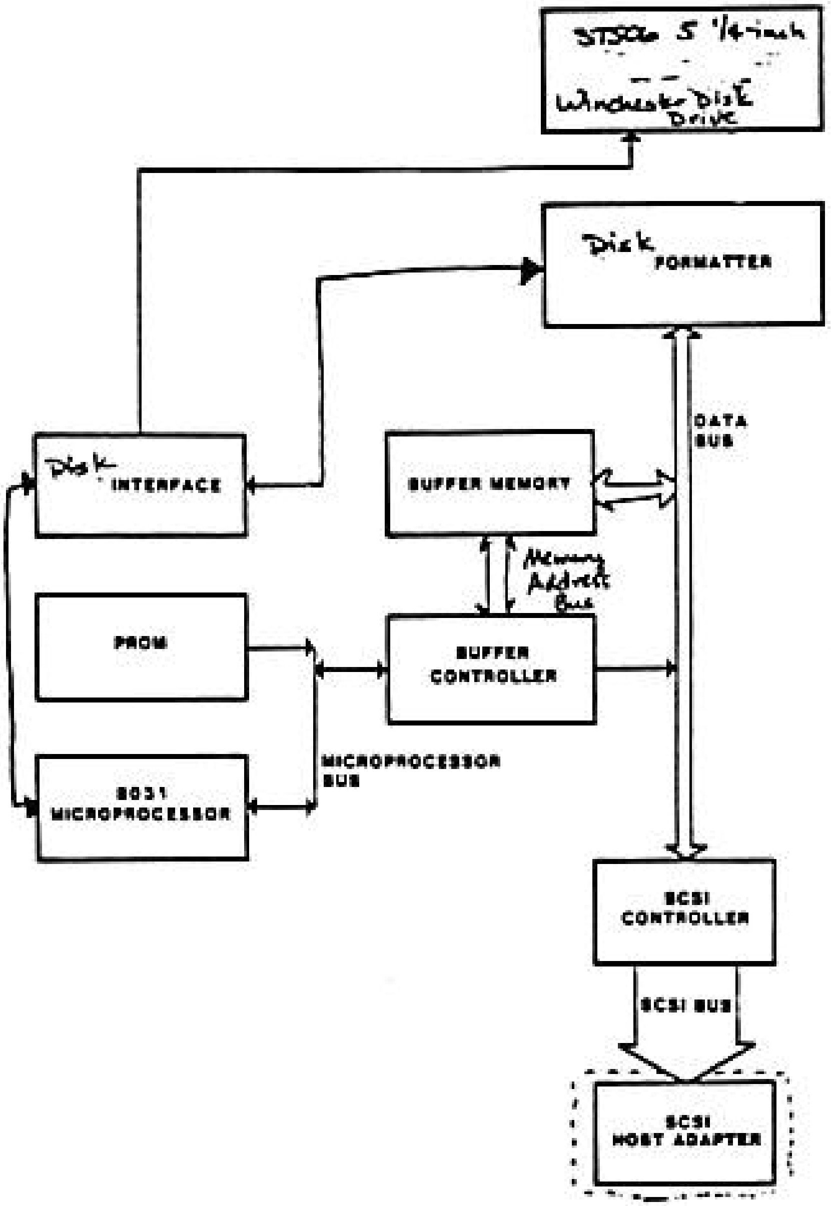


Figure 5-1. MD01 Controller Block Diagram

5.2.2 DISK FORMATTER

The Disk Formatter is a 40-pin VLSI integrated circuit fabricated with CMOS gate array technology. This circuit, in conjunction with the 8031 microprocessor, handles the read and write operations of the disk drives.

5.2.3 BUFFER CONTROLLER

The Buffer Controller is a 68-pin VLSI integrated circuit fabricated with CMOS gate array technology. The circuit is basically a three-channel DMA controller. The Buffer Controller controls data movement into or out of a dynamic buffer memory and provides the connection between the microprocessor bus and the data bus.

The Buffer Controller circuit provides the address and control for multiple MD01 Controller activities accessing a dynamic buffer memory. The Buffer Controller does the following:

- Handles addressing and control operations for the Disk Formatter
- Handles dynamic memory timing and refresh
- Performs parity checking and generation for the buffer memory
- Connects the microprocessor bus to the data bus
- Decodes the microprocessor address for the buffer memory and the internal MD01 Controller I/O space
- Determines priority of buffer memory access

3 DISK OPERATIONS

The following subsections describe MD01 Controller functions during operations with the disk drive.

5.3.1 TRACK FORMAT OPERATIONS

Each track is formatted with a physical address in the header Identification (ID) field of each sector. The MD01 Controller supports a four-byte header, shown in Figure 5-2. The track address is defined as the cylinder and head address of the specified track. Spare sectors may be allocated on each track. The interleave factor may be specified during a format operation (see the **FORMAT UNIT** command, subsection 8.3.2).

	Bit							
Byte	07	06	05	04	03	02	01	00
01	1	1	1	1	1	1	CYLN (MSB)	
02	Cylinder Number (LSB)							
03	DT	SP	Sector Number					
04	0	0	Head Number					

Figure 5-2. MD01 Controller Disk Header Format

Cylinder Number (CYLN) - Bytes 01 through 02

These bytes indicate the cylinder number of the specified track.

Defective Track (DT) - Byte 03, Bit 07

The MD01 Controller sets this bit to one when the track is defective.

Spare Sector (SP) - Byte 03, Bit 06

The MD01 Controller sets this bit to one when the sector is a spare sector on the track.

Sector Number - Byte 03, Bits <05:00>

These bits indicate the sector number.

Head Number - Byte 04, Bits <05:00>

These bits indicate the head number.

When a data track develops multiple error conditions that cannot be resolved by the use of spare sectors, the MD01 Controller reformats that data track as a flawed data track. A defective data track is reformatted with the track address of the allocated alternate track in the header of each sector. Each such header has the Defective Track bit set. The MD01 Controller does not consider the interleave factor when it formats a defective track.

An alternate track is a track in the reserved-controller storage area on the disk drive. An alternate track remains unformatted until allocated as a data storage track. When an alternate track is so allocated, it is formatted with the sector address of the defective track. The MD01 Controller considers the interleave factor when it formats an alternate track.

5.3.2 BAD SECTOR FORMAT OPERATIONS

The MD01 Controller maintains the Bad Sector File on one cylinder in an area that is not accessible to the host. The Bad Sector File is duplicated on each track of the Bad Sector File cylinder and may not be larger than one track. The Bad Sector File header format is shown below.

Byte	Bit 07 06 05 04 03 02 01 00
00	Length of Bad Sector File (Number of blocks)
01	Number of Remaining Alternate Tracks (MSB)
02	Number of Remaining Alternate Tracks (LSB)
03	Next Alternate Track Logical Block Address (MSB)
04	Next Alternate Track Logical Block Address
05	Next Alternate Track Logical Block Address
06	Next Alternate Track Logical Block Address (LSB)
07	Number of Bad Sector File Entries (MSB)
08	Number of Bad Sector File Entries (LSB)

Length of Bad Sector File - Byte 00

This byte specifies the length, in number of blocks, of the Bad Sector File, excluding the header block.

Number of Remaining Alternate Tracks - Bytes 01 through 02

These bytes specify the number of remaining Alternate Tracks on the disk drive.

Next Alternate Track Logical Block Address - Bytes 03 through 06

These bytes specify the Logical Block Address of the next Alternate Track.

Number of Bad Sector File Entries - Bytes 07 through 08

These bytes specify the total number of Bad Sector File entries.

The MD01 Controller formats data for each Bad Sector File entry in the following format:

	Bit							
Byte	07	06	05	04	03	02	01	00
9+8(n-1)	Original Logical Block Address (MSB)							
	Original Logical Block Address							
	Original Logical Block Address							
	Original Logical Block Address (LSB)							
13+8(n-1)	ALT	Re-assign Logical Block Address (MSB)						
	Re-assign Logical Block Address							
	Re-assign Logical Block Address							
	Re-assign Logical Block Address (LSB)							

where n = Bad Sector entry number

ALT Bit, Byte [13 + 8(n-1)]

When the ALT bit is set to one, the Re-assign Logical Block Address field specifies the address of the first block of the Alternate Track. When the ALT bit is reset to zero, the Re-assign Logical Block Address field specifies the Spare Logical Block Address that is equivalent to the Original Logical Block Address.

Original Logical Block Address - Bytes [9 + 8(n-1)] through [13 + 8(n-1)]

When the ALT bit is set to one, these bytes indicate the first block of the defective track. When the ALT bit is reset to zero, these bytes indicate the logical block address assigned to the Spare Logical Block Address.

Section 6
INTERFACES

6.1 OVERVIEW

This section describes the interfaces used by the MD01 Controller. It includes information about how the MD01 implements the SCSI bus interface electrical and mechanical requirements, and how it implements the ST506-compatible interface electrical requirements. This section is divided into five subsections, as listed in the following table:

Subsection	Title
6.1	Overview
6.2	SCSI Bus Interface
6.3	User's Panel Connection
6.4	DC Power Connection
6.5	Disk Drive Interface

6.2 SCSI BUS INTERFACE

Information about MD01 Controller implementation of SCSI bus electrical and mechanical requirements is provided in this subsection.

6.2.1 SCSI BUS INTERFACE PHYSICAL DESCRIPTION

SCSI bus devices are daisy chained with a common cable; both ends of the cable are terminated. All signals are common between all SCSI bus devices. The MD01 Controller supports the ANSI SCSI specification single-ended option for drivers and receivers. The maximum cable length allowed is six meters (20 feet). The length of the cable located within the FCC compliant subsystem cabinet (that contains the MD01 Controller) is included when calculating the total length of the SCSI bus. The SCSI cable that connects the compliant subsystem cabinet (that contains the MD01 Controller) to the host system must be shielded and properly grounded.

To support daisy-chain connections, SCSI devices that use shielded connectors should provide two shielded device connectors on the compliant subsystem cabinet. These two connectors may be wired one-to-one, with a stub going to the SCSI device's drivers and receivers (provided the maximum stub length specified in subsection

6.2.1.1 is not violated). Alternately, two cables may be run from two shielded connectors to the drivers and receivers so that the maximum stub length is not violated.

6.2.1.1 Internal Cable Requirements

If the MD01 Controller and the SCSI host adapter reside in the same compliant cabinet, you must use a 50-conductor flat-ribbon cable or a 25-twisted-pair flat cable to connect the MD01 Controller and SCSI host adapter. The maximum cumulative cable length is 6 meters. Each SCSI bus connection must have a 10-centimeter (4-inch) maximum stub length. For information on SCSI bus termination, see subsection 3.3.9.

6.2.1.2 Shielded Cable Requirements

If the MD01 Controller and SCSI host adapter do not reside in the same compliant subsystem, then a shielded SCSI cable must be used to connect the MD01 Controller and the host adapter. The connector for the SCSI bus shielded cable is a 50-pin connector that contains two rows of 25 female contacts on 100 mil centers. The connector shielding system must provide a direct current (DC) resistance of less than 10 milliohms from the cable shield at its termination point to the compliant subsystem cabinet. For information on FCC compliance, see subsection 3.5.

6.2.2 SCSI INTERFACE ELECTRICAL DESCRIPTION

The MD01 interfaces to SCSI host adapters and other controllers via the SCSI bus). A 50-pin male IDC connector reference designated J6 on the MD01 plugs directly into the SCSI bus. Component locations for the MD01 are shown in Figure 6-1. All signals use open collector drivers.

6.2.2.1 Output Signal Characteristics

When measured at the SCSI device's connection, each signal driven by a SCSI device has the following output characteristics:

- Signal assertion = 0.0 VDC to 0.4 VDC
- Minimum driver output capability = 48 milliamperes (sinking) at 0.5 VDC
- Signal negation = 2.5 VDC to 5.25 VDC

All assigned signals are terminated with 220 ohms to +5 volts, or 180 ohms to 4.3 VDC (nominal) and 330 ohms to ground at each end of the SCSI cable as shown in Figure 6-2.

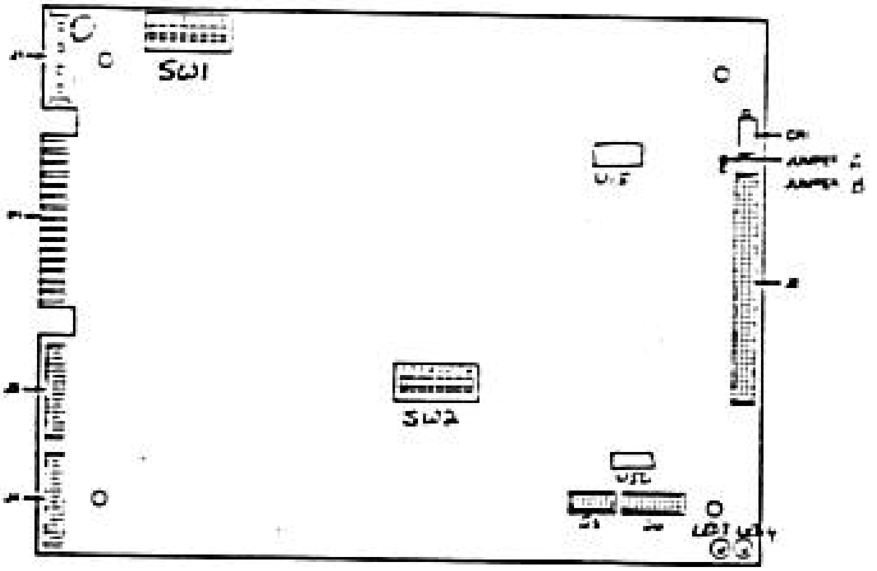


Figure 6-1. MD01 Controller Component Locations

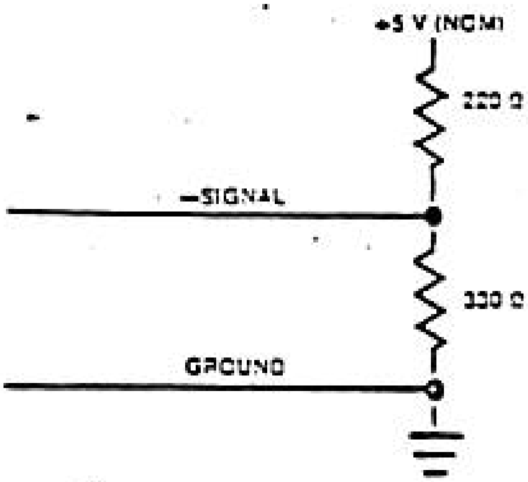


Figure 6-2. SCSI Bus Signals Termination

6.2.2.2 Input Signal Characteristics

When measured at the SCSI device's connection, each signal received by a SCSI device has the following input characteristics:

- Signal true = 0.0 VDC to 0.8 VDC
- Maximum total input load = -0.4 milliamps at 0.4 VDC
- Signal false = 2.0 VDC to 5.25 VDC
- Minimum input hysteresis = 0.2 VDC

6.2.2.3 Terminator Power (Optional)

The MD01 supports the single-ended SCSI option that provides pin 26 with termination power that has the following characteristics:

V_{CC} = 4.0 VDC to 5.25 VDC (through diode)
800 milliamps maximum source drive capability

For information on implementing the SCSI termination power option, see subsection 3.3.8.

6.2.3 SCSI BUS SIGNALS AND TIMING

SCSI bus activities involve one or more of the following SCSI phases of operation:

- Arbitration Phase
- Selection Phase
- Reselection Phase
- Command Phase
- Data Phase
- Status Phase
- Message Phase

These phases are described in Subsection 7.3. When the SCSI bus is not involved in one of the above phases, it is in the Bus Free Phase. SCSI phase sequencing is accomplished by asserting or de-asserting the SCSI bus signals; the signals are described in subsection 6.2.3.1.

6.2.3.1 SCSI Bus Signals

There are 18 signals on the SCSI bus. Nine signals are control signals that coordinate transfer of data between SCSI bus host adapters and controllers; nine signals are for an eight-bit data bus with parity. The signals are listed and described in Table 6-1.

In Table 6-1, the eight data bit signals are represented by DB0 through DB7, where DB7 is the most significant bit and has the highest priority during the Arbitration Phase. Bit number, significance, and priority decrease downward to DB0. The parity, represented by the DBP signal, is always odd. Host adapters and controllers on the SCSI bus can generate parity and have parity detection enabled. The MD01 can be configured to enable its parity detection function (see subsection 3.3.5). During the Arbitration Phase, parity is not guaranteed to be valid.

Pin/signal assignments for the SCSI bus interface are listed in Table 6-2; they support only the SCSI single-ended option.

Table 6-1. SCSI Bus Signals

Mnemonic Name	Signal	Description
DB0	Data Bus	Data Bus Bit 0
DB1	Data Bus	Data Bus Bit 1
DB2	Data Bus	Data Bus Bit 2
DB3	Data Bus	Data Bus Bit 3
DB4	Data Bus	Data Bus Bit 4
DB5	Data Bus	Data Bus Bit 5
DB6	Data Bus	Data Bus Bit 6
DB7	Data Bus	Data Bus Bit 7
DBP	Data Bus	Data Bus Parity
ACK	Acknowledge	Indicates acknowledgment for a REQ/ACK data transfer handshake operation
REQ	Request	Indicates a request for a REQ/ACK data transfer handshake operation
ATN	Attention	Indicates ATTENTION condition (i.e., the Initiator has a message to send to the Target). The ATTENTION condition is described in Subsection 7.7.2.
RST	Reset	Indicates RESET condition (i.e., clears the SCSI bus of all activity). The RESET condition is described in subsection 7.7.1.
SEL	Select	Used to select and/or reselect a SCSI bus device
BSY	Busy	Indicates the SCSI bus is being used
C/D	Control/Data	Indicates command, status information transfer, or data in and/or data out transfer
I/O	Input/Output	Indicates direction of data movement on the data bus with respect to an Initiator
MSG	Message	Indicates the SCSI bus is in the Message Phase

Table 6-2. Pin/Signal Assignments at SCSI Bus Interface

Pin	Signal Name	Input/Output
1	GND	--
2	-D0	Input/Output
3	GND	--
4	-D1	Input/Output
5	GND	--
6	-D2	Input/Output
7	GND	--
8	-D3	Input/Output
9	GND	--
10	-D4	Input/Output
11	GND	--
12	-D5	Input/Output
13	GND	--
14	-D6	Input/Output
15	GND	--
16	-D7	Input/Output
17	GND	--
18	-DP (Data parity)	Input/Output
19	GND	--
20	N/C	--
21	GND	--
22	N/C	--
23	GND	--
24	N/C	--
25	Optional GND	--
26	Optional V_{cc}	--
27	GND	--
28	N/C	--
29	GND	--
30	N/C	--
31	GND	--
32	-ATN	Input/Output
33	GND	--
34	N/C	--
35	GND	--
36	-BSY	Input/Output
37	GND	--
38	-ACK	Input/Output
39	GND	--
40	-RST	Input/Output
41	GND	--
42	-MSG	Input/Output
43	GND	--
44	-SEL	Input/Output
45	GND	--
46	-C/D	Input/Output
47	GND	--
48	-REQ	Input/Output
49	GND	--
50	-Input/Output	Input/Output

6.2.3.2 SCSI Bus Timings

Except where noted, the delay time measurements for each SCSI device (host adapter or controller) is calculated from signal conditions existing at the SCSI bus connection for that device. Normally these measurements do not consider delays in the SCSI bus cable. The SCSI timings are listed and described in Table 6-3.

The timing diagram shown in Figure 6-3, shows the typical relationship between SCSI bus signals and SCSI bus phase sequencing.

Table 6-3. SCSI Bus Timings

Timing	Duration	Description
Arbitration Delay	2.2 µsec	The minimum time a SCSI bus host adapter or controller needs from the time the -BSY signal is asserted for arbitration until the MD01 can examine the data bus to determine if arbitration has been won. There is no maximum time.
Bus Clear Delay*	800 nsec	The maximum time a SCSI bus host adapter or controller requires to stop driving all SCSI bus signals after: 1) a Bus Free Phase is detected and 2) the -SEL signal is received from another SCSI bus host adapter or controller during the Arbitration Phase.
Bus Free Delay	800 nsec	The minimum time a SCSI bus host adapter or controller waits after it has detected the Bus Free Phase until it asserts the BSY signal when going to the Arbitration Phase.

* In the Bus Clear Delay, for condition 1) the maximum time allowed for a SCSI device to clear the SCSI bus is 1200 nsec from the time the -BSY and -SEL signals both first become false. If a SCSI device requires more than a Bus Settle Delay to detect the Bus Free Phase, it clears the SCSI bus within the time duration of a Bus Clear Delay minus the excess time.

continued on next page

Table 6-3. SCSI Bus Timings (continued)

Timing	Duration	Description
Bus Set Delay	1.8 µsec	The maximum time a SCSI bus host adapter or controller is allowed after it detects a Bus Free Phase to assert the -BSY signal and the SCSI ID bit on the data bus as a requirement for entering the Arbitration Phase.
Bus Settle Delay	400 nsec	The time for the SCSI bus needs to settle after changing certain control signals.
Cable Skew Delay	10 nsec	The maximum difference allowed in propagation time between any two SCSI bus signals when measured between any two SCSI bus devices.
Deskew Delay	45 nsec	This time is used to calculate the minimum time required for deskew of certain signals.
Reset Hold Time	25 µsec	The minimum time for which the RST signal is to be asserted. There is no maximum time.
Selection Abort Time	200 µsec	The maximum timeout duration a Target (or Initiator) must take from its most recent detection of being selected (or reselected) until it asserts the BSY signal. This timeout is required to ensure a Target (or Initiator) does not assert the BSY signal after a Selection (or Reselection) Phase has been aborted. This timeout is not the same thing as the Selection Timeout Delay.
Selection Timeout Delay	250 msec	The minimum recommended time an Initiator (or Target) should wait for a -BSY response, during the Selection or Reselection Phase, before starting the timeout procedure.

msec = milliseconds
µsec = microseconds
nsec = nanoseconds

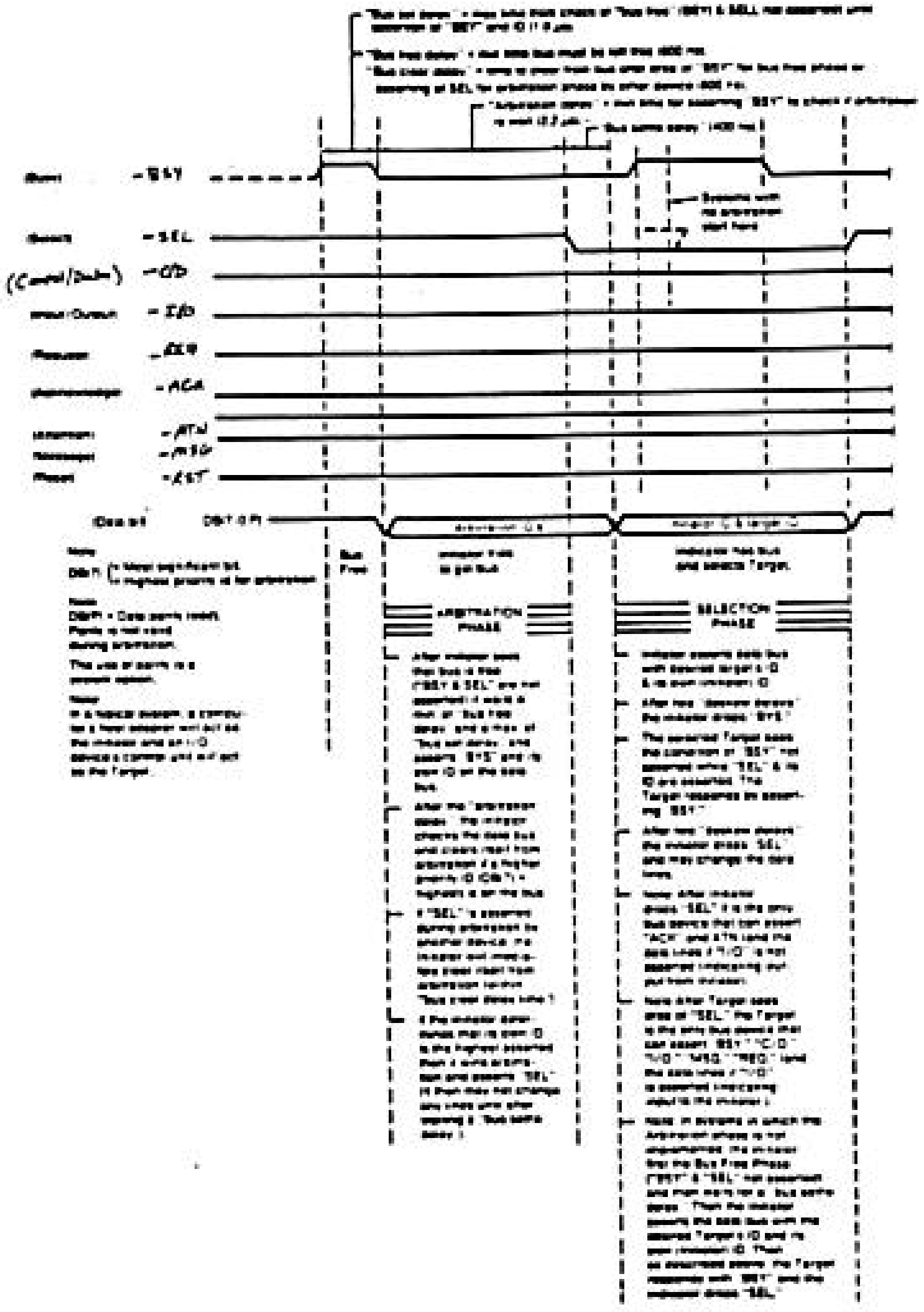
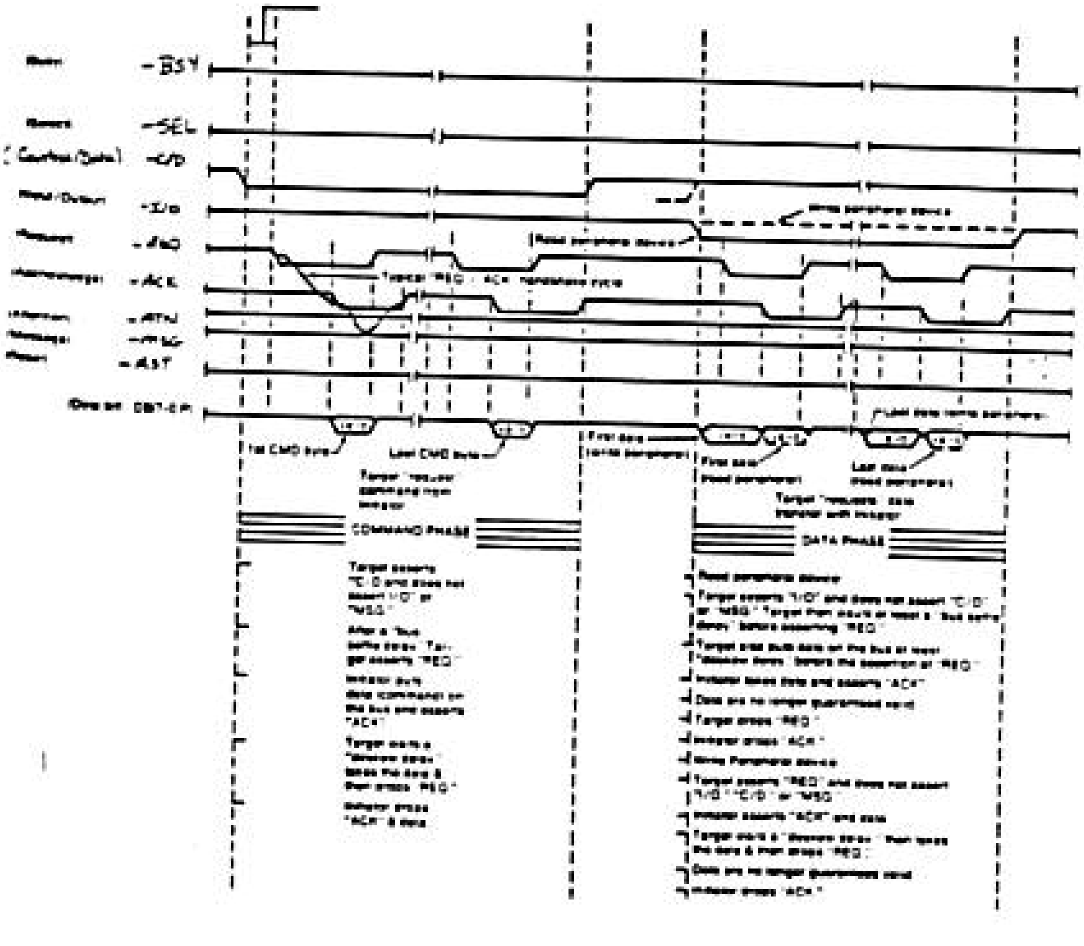


Figure 6-3. SCSI Bus Timing Diagram (Sheet 1 of 3)


Busy -BSY
Select -SEL
(Control/Data) -C/D
Input/Output -I/O
Request -REQ
Acknowledge -ACK
Attention -ATN
Message -MSG
Reset -RST
Data bit DB7-0,P
Typical "REQ" / "ACK" handshake cycle
Read peripheral device
Write peripheral device
1st CMD byte
Last CMD byte
Target "requests" command from initiator
First data (write peripheral)
First data (read peripheral)
Last data (read peripheral)
Last data (write peripheral)
Target "requests" data transfer with initiator
COMMAND PHASE
DATA PHASE

Target asserts "C/D" and does not assert "I/O" or "MSG."

After a "bus settle delay," Target asserts "REQ."

Initiator puts data (command) on the bus and asserts "ACK."

Target waits a "deskew delay," takes the data & then drops "REQ."

Initiator drops "ACK" & data.

Read peripheral device

Target asserts "I/O" and does not assert "C/D" or "MSG." Target then waits at least a "bus settle delay" before asserting "REQ."

Target puts data on the bus at least "deskew delay" before the assertion of "REQ."

Initiator takes data and asserts "ACK."

Data are no longer guaranteed valid

Target drops "REQ."

Initiator drops "ACK."

Write Peripheral device

Target asserts "REQ" and does not assert "I/O," "C/D" or "MSG."

Initiator asserts "ACK" and data

Target waits a "deskew delay," then takes the data & then drops "REQ."

Data are no longer guaranteed valid

Initiator drops "ACK."

Figure 6-3. SCSI Bus Timing Diagram (Sheet 2 of 3)

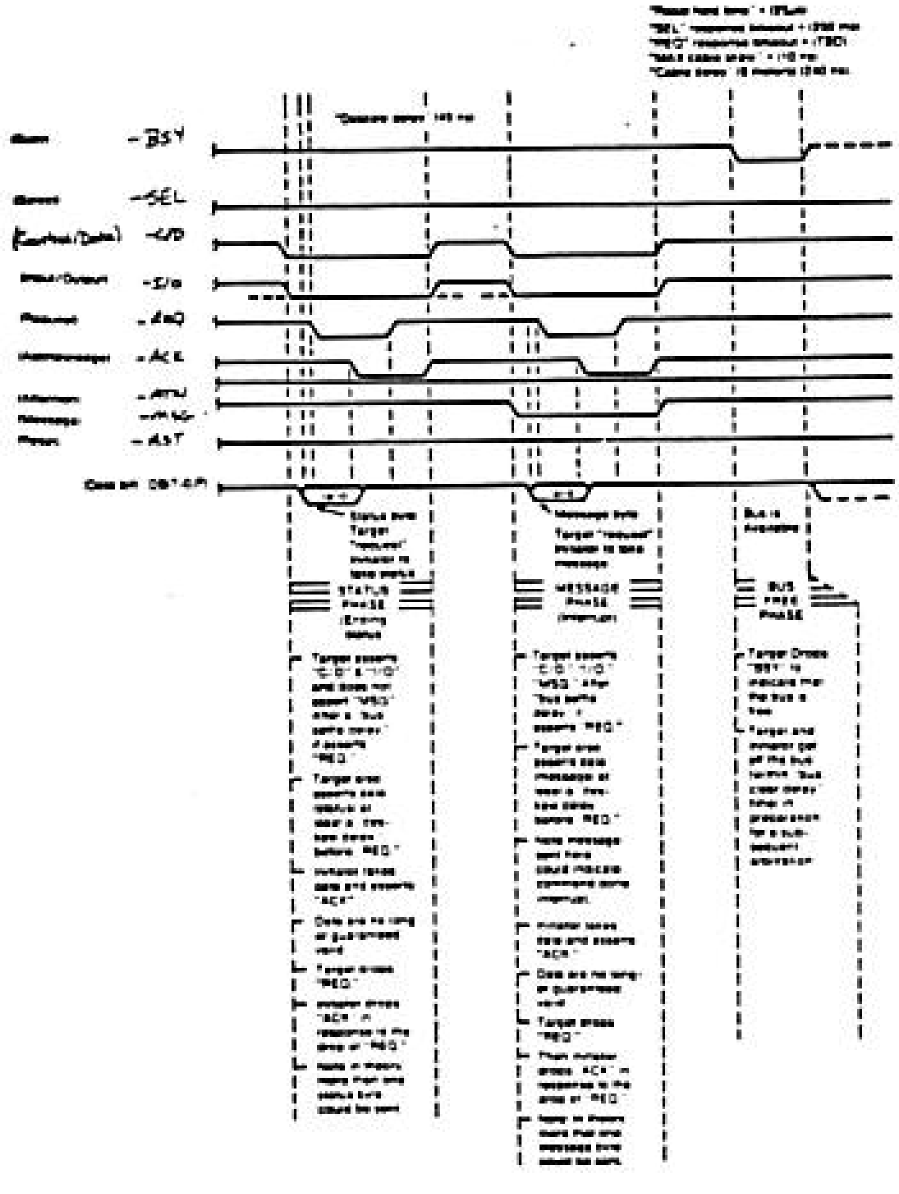


Figure 6-3. SCSI Bus Timing Diagram (Sheet 3 of 3)

6.3 MD01 CONTROLLER USER'S PANEL CONNECTION

Connector J5 (see Figure 6-1) on the MD01 Controller is called the user's panel connector. It is used to connect the MD01 Controller to external LEDs. On Emulex subsystems, these external LEDs are located on the user's panel resident on the subsystem bezel. The user's panel connector is a 10-pin 3M P/N 3473-XXXX. The connector pin descriptions are listed in Table 6-4 and described in this subsection.

Table 6-4. Connector J5 Pin Description

Pin	Connection	True	Function
1	Ground	--	--
2	--	--	--
3	SW3	High	Drive 1 Write Protect
4	LED 4	Low	Drive 1 Ready
5	SW2	High	Drive 0 Write Protect
6	LED 3	Low	Drive 0 Ready
7	LED 2	Low	Drive 1 Write Protect On
8	SW1	High	Not Used
9	LED 1	Low	Drive 0 Write Protect On
10	+5 volts	--	

LED 0 Ready - When the low level is applied to this signal line, LED 0 is lit to indicate Disk Drive 0 is in the online mode and not busy.

LED 1 Write Protect On - When the low level is applied to this signal line, LED 1 is lit to indicate Disk Drive 0 is write protected.

LED 2 Ready - When the low level is applied to this signal line, LED 2 is lit to indicate Disk Drive 1 is in the online mode and not busy.

LED 3 Write Protect On - When the low level is applied to this signal line, LED 3 is lit to indicate Disk Drive 1 is write protected.

6.4 DC POWER CONNECTION

The MT01 Controller power supply, reference designated J1 (see Figure 6-1), is an AMP P/N 641737-1. Table 6-5 lists the power connections for this connector. The pin locations for this connector are shown in Figure 6-4.

Table 6-5. Power Supply Connections at Connector J1

Pin	Description
1	No Connection
2	No Connection
3	Ground
4	+5 VDC, ± 5%, 1.5 amps nominal

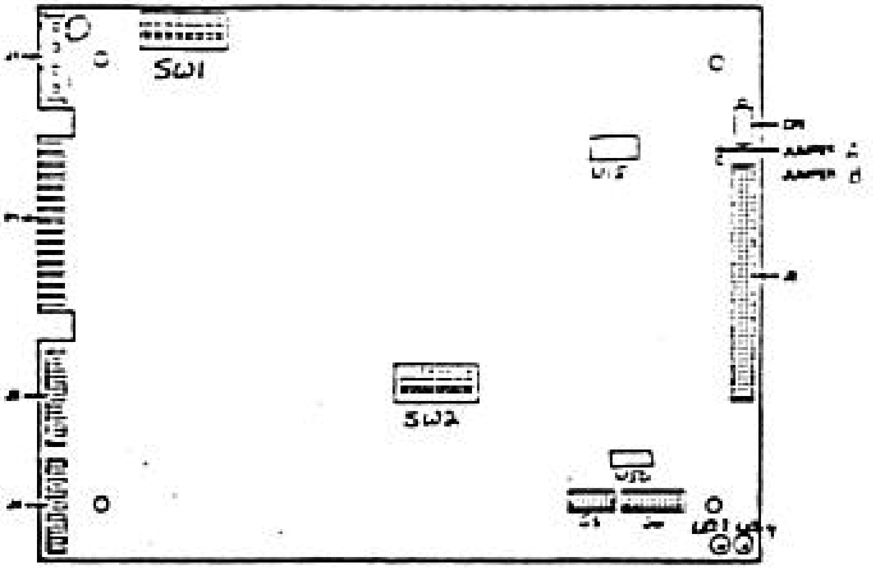


Figure 6-4. Pin Locations for Connector J1

6.5 DISK DRIVE INTERFACE

The MD01 Controller interfaces with ST506 disk drives via a 34-pin control cable and a 20-pin data cable, for each disk drive. A 34-pin male connector at reference designator P1 on the MD01 Controller plugs directly into the ST506 disk drive control cable. The MD01 Controller contains two 20-pin male connectors, one at reference designator J3 and one at reference designator J4. The MD01 Controller can integrate a maximum of two disk drives. Either 20-pin connector (reference designator J3 or J4) can plug directly into the data cable for the first disk drive. If a second disk drive is configured, the unused 20-pin connector is plugged into the data cable for that disk drive.

The pin/signal assignments for control signal interface between the MD01 Controller and an ST506 disk drive are shown in Figure 6-4. The pin/signal assignments for data signal interface between the MD01 Controller and an ST506 disk drive are shown in Figure 6-5.

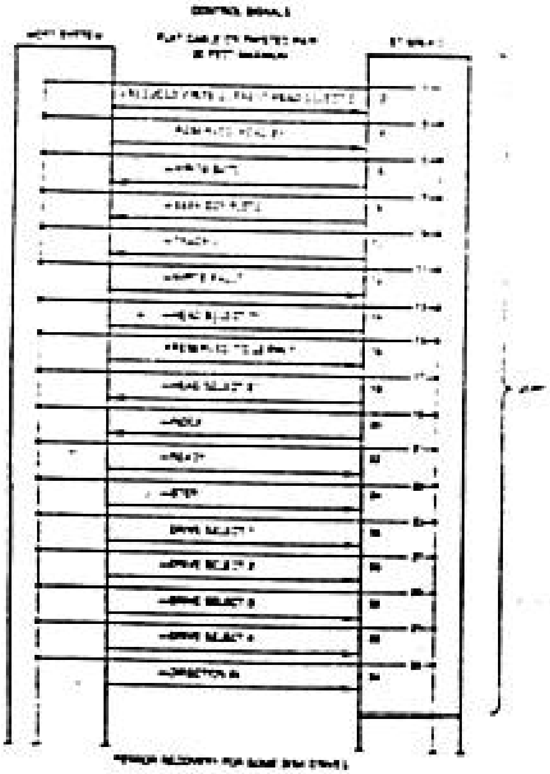


Figure 6-5. Control Pin/Signal Assignments at ST506 Disk Drive Interface (Connector P1)

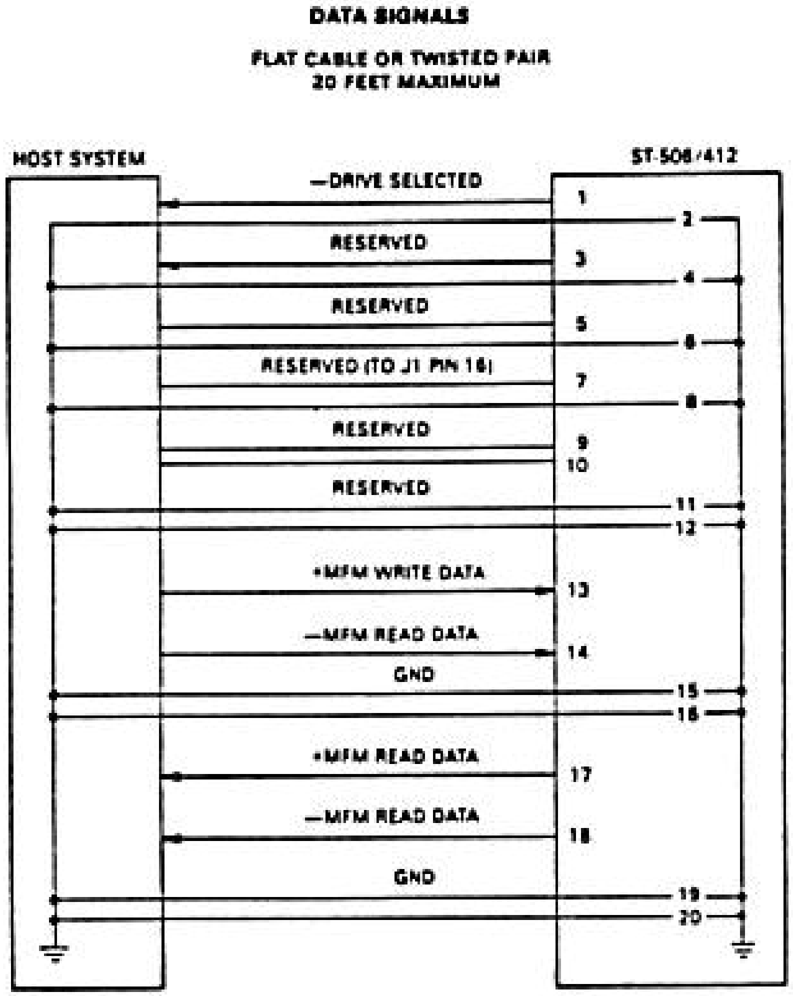


Figure 6-6. Data Pin/Signal Assignments at ST506 Disk Drive Interface (Connector J3 or J4)

7.1 OVERVIEW

This section describes the SCSI bus protocol. It includes information on SCSI bus phases and phase sequencing, procedures for queuing SCSI bus commands, and procedures for passing control and status information between SCSI bus host adapters and controllers by using SCSI memory address pointers. This section is divided into seven subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	SCSI Bus Overview
7.3	SCSI Bus Phases
7.4	SCSI Bus Phase Sequencing
7.5	SCSI Memory Address Pointers
7.6	SCSI Bus Conditions

7.2 SCSI BUS DESCRIPTION

The Small Computer System Interface (SCSI) is a standard interface established to support mass storage, printer output, and network communication for microcomputers and minicomputers. The interface is an eight-port, daisy-chained bus. The SCSI command standard for the MD01 Controller is based on the ANSI X3T9.2/82-2 Revision 14 (01 May 1984) SCSI Interface Specification.

The SCSI bus can support up to eight SCSI host adapters and/or controllers. Each controller can be connected to a maximum of eight devices (called Logical Unit Numbers, or LUNs). The MD01 Controller hardware supports any combination of host adapters, intelligent controllers, or intelligent peripherals connected to the SCSI bus. The MD01 Controller supports up to two LUNs (ST506-compatible disk drives). Three basic SCSI configurations are supported with the MD01 Controller and SCSI bus:

- Single initiator, single target
- Single initiator, multi target
- Multi initiator, multi target

Communication on the SCSI bus occurs between a host adapter and a controller. (The MD01 Controller also supports communication between two controllers, as in a copy operation.) When a host adapter and a controller communicate, one acts as the Initiator and the other acts as the Target. The Initiator (usually the host adapter) originates an operation, and the Target (usually a peripheral controller, such as the MD01 Controller) performs the operation. Sample system configurations supported by MD01 Controller hardware are shown in Figure 7-1.

Some SCSI bus functions are assigned to the Initiator and some functions are assigned to the Target. The Initiator can arbitrate for control of the SCSI bus and select a specific Target. The Target can request the transfer of command, data, status, or other information via the SCSI bus. In some circumstances, the Target can arbitrate for control of the SCSI bus to reselect an Initiator and continue an operation. Sometimes, the Target becomes an Initiator and arbitrates for control of the SCSI bus; for example, when it performs a copy operation.

SCSI bus data transfer operations are asynchronous and follow a defined request/acknowledge (REQ/ACK) handshake protocol. (This protocol is defined in the ANSI SCSI specification.) One eight-bit byte of information can be transferred with each handshake.

The SCSI bus consists of 18 signal lines. Nine signal lines are for an eight-bit data bus with parity; the other nine signal lines are for control and status signals that coordinate data transfer operations between the host adapter and SCSI controllers. SCSI bus signals are described in detail in subsection 6.2.3.1.

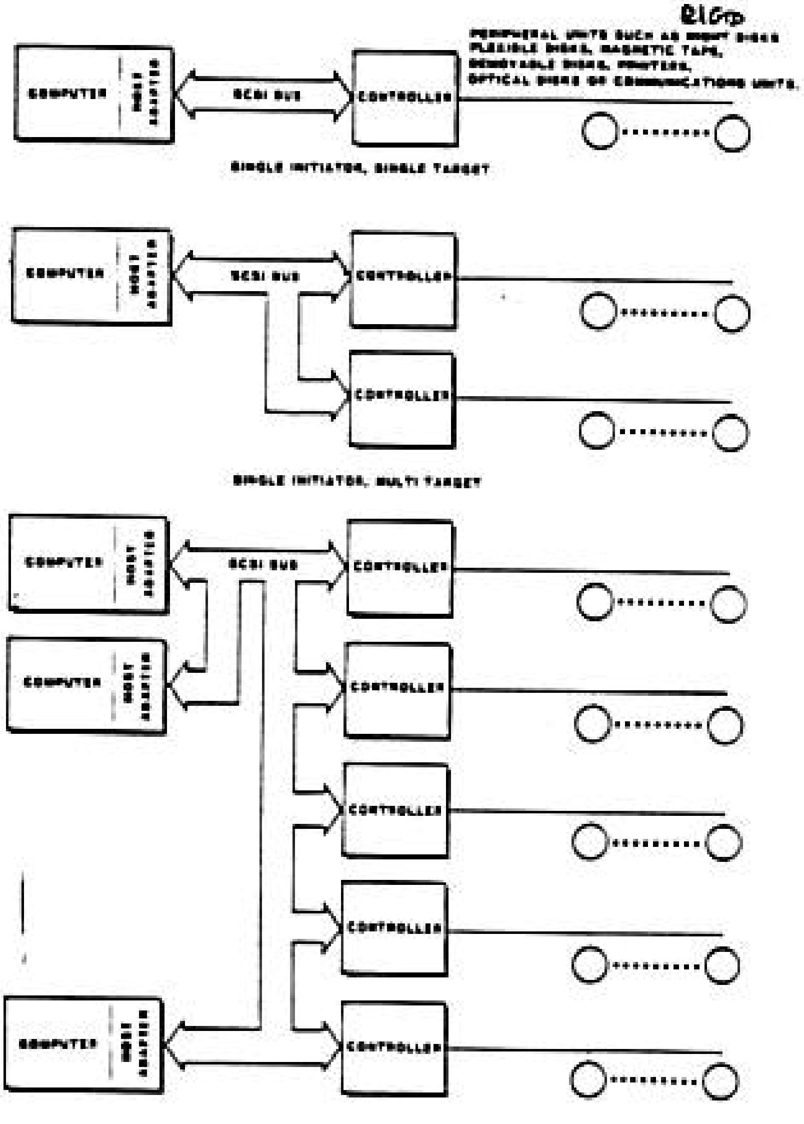


Figure 7-1. Sample SCSI Bus Configurations

7.3 SCSI BUS PHASES

The activities on the SCSI bus can be divided into the following phases of operation:

- Arbitration
- Selection
- Reselection
    - Command
    - Data
    - Status
    - Message

These phases are supported as specified by the ANSI SCSI specification (listed in subsection 1.1.1). The phases are individually discussed in subsequent subsections. The last four phases (Command, Data, Status, and Message) are grouped together as Information Transfer Phases.

When the SCSI bus is not involved in one of the SCSI bus phases, it is in a Bus Free Phase. The Bus Free Phase indicates that no host adapter or controller is actively using the SCSI bus and the SCSI bus is available for subsequent users.

The SCSI bus activities, implemented by the MD01 Controller, include the disconnect function (see subsection 1.3) and reselection function (see subsection 7.3.2). Overlapped operations on multiple controllers and multiple logical units are supported.

In the following subsections, no attempt is made to detail the SCSI bus signal sequences; the signals are listed in subsection 6.2.3.1. If detailed signal sequence information is required, refer to the ANSI SCSI standard listed in subsection 1.1.1.

7.3.1 ARBITRATION PHASE

The Arbitration Phase is an optional implementation on the SCSI bus. This phase is used when multiple controllers or processors vie for SCSI bus ownership. Since multiple hosts adapters and/or controllers may desire control of the SCSI bus concurrently, arbitration for the SCSI bus is a requirement for the MD01 Controller.

7.3.2 SELECTION AND RESELECTION PHASES

The SCSI bus Selection and Reselection phases provide methods for establishing a link between the Initiator and a desired Target.

Usually the MD01 Controller is selected by an Initiator to perform some function (e.g., read or write data). The MD01 Controller then has the option of disconnecting from the SCSI bus. When the MD01 Controller needs to re-establish the link to its original Initiator, it reselects that Initiator.

For the copy function, however, the MD01 Controller can behave as an Initiator and select another controller as a Target source or destination for the copy operation. While in the Initiator mode, the MD01 Controller always issues an IDENTIFY message (see subsection 7.3.3.4) after selecting a Target.

The SCSI Selection and Reselection Phases can be terminated for any one of three conditions:

1. The preceding Selection or Reselection Phase is successfully completed by using the Selection/Reselection handshake protocol.
2. A Selection/Reselection timeout occurs. The timeout results if any Target or Initiator does not respond to the Selection/Reselection Phase within a timeout period of two seconds.
3. A Reset (-RST) signal occurs on the SCSI bus. When this signal is asserted, all SCSI bus sequences are immediately terminated and the SCSI bus signals are released by all Initiators and Targets.

The Initiator can use the Attention (-ATN) signal to notify the MD01 Controller that a message from the Initiator is ready. To guarantee that the Target recognizes the Attention condition before the Command Phase is entered, the -ATN signal level must be true before the Selection or Reselection Phase is completed.

If an IDENTIFY message is used during the Selection Phase sequence, the specified Logical Unit Number (LUN) has precedence over the LUN field in the Command Descriptor Block (CDB). (CDBs are described in detail in Section 8.) The IDENTIFY message also informs the Target if the Initiator supports the disconnect function.

NOTE

> If the Initiator selects a nonexistent LUN, a vendor unique status of nonexistent device (NED bit) is returned in the Status Byte (see Subsection 7.3.3.3.1). Selected LUNs that have not been initialized by the MD01 Controller report a BUSY status code (e.g., at startup, or when they are not connected to the MD01 Controller).

7.3.3 INFORMATION TRANSFER PHASES

The Command, Data, Status, and Message Phases are grouped together as Information Transfer Phases because they are all used to transfer data or control information via the SCSI data bus. The Information Transfer Phases are described in the following subsections.

7.3.3.1 Command Phase

The Command Phase allows the Target to request command information from the Initiator. An Initiator issues SCSI commands to a Target by transferring a command packet, called a Command Descriptor Block (CDB). The length of the SCSI command and the meaning of the information in the command packet depends on which command is being transferred. (See Section 8 for definitions of SCSI commands and all SCSI CDBs supported by the MD01 Controller.)

The last byte of every command packet (see Figure 8-1) is a control byte and can be differentiated into the following bit groups:

- The low-order two bits control the ability to link commands in a sequence and to notify the host adapter when a particular command (CDB) step is completed. These two bits are designated Flag and Link in the descriptions of MD01 Controller command packets in Section 8.
- The remaining bits in the control byte are reserved bits, and are always zero.

The remainder of the bytes of the command packet are primarily command-dependent.

The Command Phase is interrupted only for the following exception conditions:

- **Reset Condition.** This condition can occur when the SCSI Reset (-RST) signal is asserted or a power fail or power-off condition in the Target occurs. In this case, the Command Phase and the connection established during the Selection/Reselection Phase is terminated by the Target with the release of the -BSY signal.

- **Parity Error Condition.** The Target detects a parity error on the SCSI bus during the command transfer operation. At this time, the MD01 Controller releases the -BSY signal, terminates the connection, and the SCSI bus returns to the Bus Free phase.

7.3.3.2 Data Phase

The Data Phase of a connection controls the transfer of data between the Initiator and Target devices. The Data Phase includes both the Data In Phase and the Data Out Phase. The Data In Phase allows the Target to request sending of data to the Initiator from the Target. The Data Out Phase allows the Target to request sending of data to the Target from the Initiator. The direction of the data transfer operation depends on the command being processed. Some commands may have no data to be transferred and therefore have a null Data Phase. Only the asynchronous data transfer mode is supported by the MD01 Controller.

The Data Phase is interrupted only for the following exception conditions:

- **Reset Condition.** This condition can occur when the SCSI Reset (-RST) signal is asserted or when a power fail or power-off condition in the Target occurs. In this condition, the Data Phase and the connection established during the Selection/Reselection Phase are terminated by the Target with the release of the -BSY signal.
- **Data Out Parity Error Condition.** The Target detects a parity error on the SCSI bus during the data transfer operation from the Initiator to the Target.
- **Data In Parity Error Condition.** The Initiator detects a parity error on the SCSI bus during the data transfer operation from the Target to the Initiator. The Initiator can then assert the -ATN signal along with the Acknowledge (-ACK) signal. The Target detects this condition and enters the message out phase to receive a message. The Initiator sends an Initiator-detected error message in response.

7.3.3.3 Status Phase

The Status Phase is used by the Target to send completion information to the Initiator. The status is sent in a single byte, the format of which is defined in subsection 7.3.3.3.1.

The Target can initiate the Status Phase when any one of the following conditions occur:

- **Busy Status.** The Selection Phase is completed and the Target is in a BUSY state and unable to process any commands for an extended period of time. The Target can initiate the Status Phase immediately after this condition occurs. The Status Byte transferred has the BUSY status code set.
- **Reservation Conflict Status.** The Command or Reselection Phase is completed and the specified LUN is reserved for another Initiator. The Status Byte transferred has the RESERVATION CONFLICT status code set.
- **Terminated Status.** At the termination of a command, the Status Byte transferred has the GOOD STATUS code set to indicate the success of the command.

NOTE

In multi-Initiator environments, the Initiator delays a minimum of 200 microseconds before attempting another selection of a Target if a BUSY status code for that Target is received.

7.3.3.3.1 Status Byte Format. The format of the Status Byte used by the Target to send completion information to the Initiator is defined below.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	Status Code				NED

Status Code - Bits <04:01>

These bits are used to specify the status code. Table 7-1 lists and describes the status codes.

Nonexistent Device (NED) - Bit 00

When the NED bit is set to one, the Initiator selected a LUN that is not configured in the system.

Table 7-1. Status Codes

Bits 04 03 02 01	Status	Description
X 0 0 0	GOOD STATUS	The MD01 Controller successfully completed the command.
0 0 0 1	CHECK CONDITION	An error, exception, or abnormal condition occurred.
0 1 0 0	BUSY	The MD01 Controller is busy.
1 0 X 0	INTERMEDIATE STATUS	Sent for every command in a series of linked commands (see subsection 7.3.3.1) unless a CHECK CONDITION or RESERVATION CONFLICT status code is detected.
1 1 0 0	RESERVATION CONFLICT	Sent to an Initiator that attempts to access a LUN connected to the MD01 Controller when another Initiator has reserved the LUN.
1 = Set	0 = Cleared	X = Don't Care

7.3.3.4 Message Phase

The Message Phase is used to transfer information about exception conditions between the Initiator and the Target. The Message Phase includes both the Message In and the Message Out Phases. The Message In Phase allows a Target to request that messages be sent to the Initiator from the Target. The Message Out Phase allows a Target to request that messages be sent from the Initiator to the Target. Messages from the MD01 Controller are a single byte in length; they (and their corresponding hexadecimal codes) are listed and described in Table 7-2.

Table 7-2. MD01 Controller SCSI Messages

Code	Message	Description
00	COMMAND COMPLETE	Issued by the Target just before releasing the -BSY signal at the end of a command execution. This message is generally sent immediately after a Status Phase.
02	SAVE DATA POINTER	Issued by the Target to direct the Initiator to save a copy of the present active data pointer. This message is issued just before the MD01 Controller issues the DISCONNECT message and disconnects from the bus.
04	DISCONNECT	Issued by the Target just before releasing the -BSY signal to indicate to the Initiator that the present physical connection is temporarily broken. The current data, command, and status pointers are not saved.
05	INITIATOR DETECTED ERROR	Issued by an Initiator to inform the Target that an error has occurred during a read operation.
06	ABORT	Issued by the Initiator to the Target to clear the specified LUN and cause the SCSI bus to go to the Bus Free Phase.
07	MESSAGE REJECT	Issued by the Initiator or Target in response to a received message that was undefined.
08	NO OPERATION	A null message issued by the Initiator if the Target requests a message from the Initiator but the Initiator has no message to convey.
09	MESSAGE PARITY ERROR	Issued by the Initiator to inform the MD01 Controller that a parity error has occurred on a message receive operation from the Target to the Initiator. The MD01 attempts to send the message one more time.

continued on next page

Table 7-2. MD01 Controller SCSI Messages (continued)

Code	Message	Description
0A	LINKED COMMAND COMPLETE	Issued by the Target to the Initiator to indicate the completion of a linked command (see subsection 7.3.3.1).
0B	LINKED COMMAND COMPLETE WITH FLAG	Issued by the Target to the Initiator to indicate the completion of a linked command that had the Flag bit set.
0C	BUS DEVICE RESET	Issued by the Initiator to the Target to reset all current I/O activities on the SCSI bus MD01 Controller. This message generates a hard Reset Condition (see subsection 7.7.1).
80-FF	IDENTIFY *	Issued by the Target or Initiator to establish a connection to a particular LUN. The following bits have particular meaning: Bit 07 - Always set to one. Bit 06 - Set if the Initiator can support Disconnect and Reconnect sequences. Bits <02:00> - Specify LUN address (hexadecimal) in a Target.

* If the disconnect function is supported, this message is issued to the MD01 Controller at the beginning of every command sequence.

7.4 SCSI BUS PHASE SEQUENCING

The status of the SCSI bus is a function of the control signals. (The control signals are described in subsection 6.2.3.) These signals place the SCSI bus in one of four phases: Arbitration, Selection/Reselection, Information Transfer, or Bus Free (see subsection 7.3). The order in which SCSI bus phases are used follows the prescribed sequence shown in Figure 7-2.

All SCSI command sequences start with the Bus Free Phase. The normal progression is from the Bus Free Phase to the Arbitration Phase. During arbitration, host adapters or controllers contest for control of the SCSI bus; priority is given to the contestant that has the highest SCSI bus address.

SCSI Bus Phase Sequencing

Once a host adapter or controller has control (i.e., is the bus master) of the SCSI bus, the SCSI bus enters the Selection/Reselection Phase. This phase allows the bus master to select a specific device for communication. An Initiator can select a Target to initiate an operation, or a Target can reselect an Initiator to continue an operation.

After a physical path between an Initiator and a Target is established, the SCSI bus enters one of the Information Transfer Phases. These phases include six types of information exchange:

- Data Out Phase
- Data In Phase
- Command Phase
- Status Phase
- Message In Phase
- Message Out Phase

These types of SCSI bus information exchange are described in more detail in subsection 7.3.

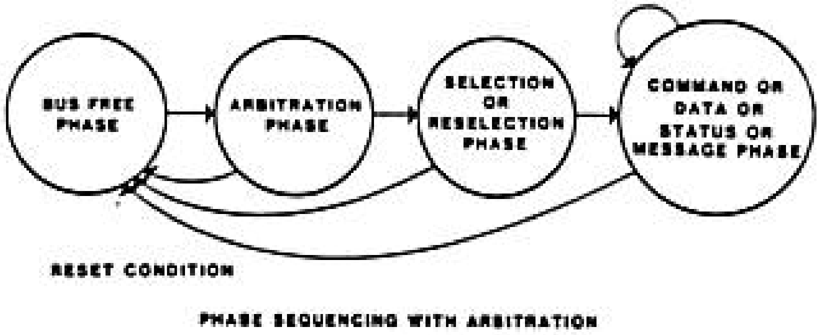

BUS FREE PHASE
ARBITRATION PHASE
SELECTION OR RESELECTION PHASE
COMMAND OR DATA OR STATUS OR MESSAGE PHASE
RESET CONDITION
PHASE SEQUENCING WITH ARBITRATION

Figure 7-2. SCSI Bus Phase Sequences

7.5 SCSI MEMORY ADDRESS POINTERS

There are three "conceptual" memory address pointers, located in host adapter memory, that point to the next byte of command, data, or status information to be accessed. The pointers are used to represent the state of the interface. After the pointers are initially loaded by the Initiator, their movement is under control of the Target. When the Target transfers a byte of information to or from one of the three pointers, the position of that pointer is incremented.

The SCSI command set is independent of the types of host adapters and peripheral device controllers (tape drives or disk drives) attached to the SCSI bus. The SCSI command set masks the internal structure of the device (cylinders, tracks, sectors, data blocks, etc.) from the SCSI bus. The SCSI command set supported by the MD01 Controller is defined in Section 8. The host memory contains three I/O blocks: command, data, and status. During SCSI bus I/O operations, the MD01 Controller initially reads a command block located in host memory to determine the I/O task to be performed. The MD01 Controller then reads from, or writes to, a host memory data block as an I/O task proceeds. At the end of an I/O operation, the MD01 Controller writes to a status block (in host memory).

There are two sets of three pointers within the host adapter. The first set, the Current Pointer Values, addresses the next command, status, or data byte to be transferred to the MD01 Controller. The second set, the Saved Pointer Values, always addresses the start of the command and status block, but increments for the data block.

During a disconnect operation, the MD01 Controller enters the Message Phase and issues a SAVE DATA POINTER message to the Initiator.

7.6 SCSI BUS CONDITIONS

The SCSI bus has the following asynchronous conditions:

- Reset Condition
- Attention Condition

These conditions cause certain SCSI device actions and can alter the phase sequence. The two conditions are described in the following subsections.

7.6.1 RESET

The Reset Condition is used to immediately clear all bus masters from the SCSI bus. This condition takes precedence over all other SCSI bus phases and conditions. During the Reset Condition, no SCSI bus signal except -RST is guaranteed to be valid.

The MD01 Controller supports the SCSI Hard Reset option (the SCSI Soft Reset option is not supported). When it detects a Reset Condition, the MD01 Controller performs the following event sequence:

- Clears all uncompleted commands
- Releases device reservations
- Returns device operating modes (such as the **MODE SELECT** command) to their default conditions

The Hard Reset condition has the same effect on the MD01 Controller as power-on; therefore, all Initiator-defined parameters must be re-submitted to the MD01 Controller.

7.6.2 ATTENTION

The Attention Condition allows an Initiator to inform a Target that the Initiator has a message ready. The Target can obtain this message in the Message Phase.

Section 8
SCSI COMMAND SET

8.1 OVERVIEW

This section describes the SCSI commands supported by the MD01 Controller and it is divided into five subsections, as listed in the following table:

Subsection	Title
8.1	Overview
8.2	SCSI Command Descriptor Block Structure
8.3	SCSI Group Code 0 Command Descriptions
8.4	SCSI Group Code 1 Command Descriptions
8.5	SCSI Group Code 6 Command Descriptions

.2 SCSI COMMAND DESCRIPTOR BLOCK STRUCTURE

An Initiator issues SCSI commands to a Target device by transferring a command packet, called a Command Descriptor Block (CDB). The command contained in the CDB determines the length of the CDB. The first byte of a CDB contains the command. This byte, called the Operation Code, has two components: the Group Code and the Command Code.

Only Group Code 0, Group Code 1, and Group Code 6 commands are acceptable to the MD01 Controller. Group Code 0 CDBs contain six bytes (see subsection 8.3). Group Code 1 and Group Code 6 CDBs contain ten bytes; they are described in subsections 8.4 and 8.5 respectively. The Command Code defines the type of SCSI command. SCSI command types are defined as specific CDB bit patterns in the ANSI SCSI specification; CDBs supported by the MD01 Controller follow the guidelines listed in the ANSI SCSI specification.

The structure of each SCSI Group Code 0 command packet that can be accepted by the MD01 Controller is shown in the applicable descriptions in subsection 8.3. The structure of each SCSI Group Code 1 command packet acceptable to the MD01 Controller is shown in the individual command packet descriptions in subsection 8.4. The structure of each SCSI Group Code 6 command packet that is acceptable to the MD01 Controller is shown in the individual descriptions in subsection 8.5. The following table lists, by subsection number, command names and operation codes for SCSI commands supported by the MD01 Controller:

Subsection	MD01 SCSI Command	Code
8.3.1	COPY	18
8.3.2	FORMAT UNIT	04
8.3.3	INQUIRY	12
8.3.4	MODE SELECT	15
8.3.5	MODE SENSE	1A
8.3.6	READ	08
8.4.2	READ (EXTENDED)	28
8.4.1	READ CAPACITY	25
8.5.1	READ LONG	E8
8.3.7	RE-ASSIGN BLOCK	07
8.3.8	RECEIVE DIAGNOSTIC	1C
8.3.9	RELEASE UNIT	17
8.3.10	REQUEST SENSE	03
8.3.11	RESERVE UNIT	16
8.3.12	REZERO UNIT	01
8.4.3	SEARCH DATA EQUAL	31
8.4.4	SEARCH DATA HIGH	30
8.4.5	SEARCH DATA LOW	32
8.3.13	SEEK	0B
8.4.6	SEEK (EXTENDED)	2B
8.3.14	SEND DIAGNOSTIC	1D
8.4.7	VERIFY	2F
8.3.15	TEST UNIT READY	00
8.3.16	WRITE	0A
8.4.8	WRITE (EXTENDED)	2A
8.4.9	WRITE AND VERIFY	2E
8.5.2	WRITE LONG	EA

8.3 SCSI GROUP CODE 0 COMMAND DESCRIPTIONS

This subsection provides detailed descriptions of SCSI Group Code 0 commands, including CDB formats, hexadecimal operation code, byte and bit functions, and any necessary effects produced by the commands. Each SCSI command is described in a separate subsection.

A sample Group 0 CDB is shown in Figure 8-1. The first byte of a command (Byte 00) contains two fields: the Group Code in the high-order three bits (bits <07:05>), and the Command Code in the low-order five bits (bits <04:00>). The Group Code determines the length of the command packet in the CDB, and together the Group and Operation Codes determine the operation to be performed.

Bits <07:05> of byte 01 in the CDB contain the LUN of the device being addressed. The MD01 Controller, acting as a SCSI bus Target, supports up to two LUNs (ST506-compatible disk drives). Therefore, the value for the LUN field in byte 01 in the CDB is usually 000 or

001. The LUN must be specified for all commands. If a LUN value issued by the Initiator in an IDENTIFY message differs from the value specified in the CDB, that value supersedes the value specified in the CDB. The definition of the low-order bits in byte 01 is based on the current command.

The last byte (byte 05) in every CDB is a Control Byte, which is differentiated into two groups:

- The low-order two bits control the ability to link commands in a sequence and to notify the host adapter that a particular command (CDB) step has been completed. These two bits are designated Flag and Link in the descriptions of command packets presented in this subsection for the MD01 Controller.

- The remaining bits in the Control Byte indicate whether the Error Retry, ECC Checking, and Alternate Vectoring operations are disabled or not.

The remaining bytes in the CDB are primarily command-dependent.

NOTE

> If a byte in a CDB can be any bit pattern, it is specified as **Not Used** in the paragraphs describing that CDB. If a byte in a CDB must be all zeros, it is specified as **Reserved** in the paragraphs describing that CDB.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	Group Code			Command Code				
01	LUN			Command-Dependent Parameters				
02	Command-Dependent Parameters							
03	Command-Dependent Parameters							
04	Command-Dependent Parameters							
05	0	0	0	0	0	0	Flag	Link

Figure 8-1. Sample Group 0 Command Descriptor Block

8.3.1 COPY 18

The COPY CDB, shown below, causes large amounts of data to be moved from one peripheral device to another. The data transfer operation occurs off-line and is performed without Initiator resources.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	0	0
01	LUN			0	0	0	0	0
02	Length of Parameter List (MSB)							
03	Length of Parameter List							
04	Length of Parameter List (LSB)							
05	0	0	0	0	0	0	Flag	Link

An external device controller may be specified as either the source device or destination device, but at least one device must be internal to the MD01 Controller. If an external device is specified as a source or destination and the host adapter does not support the disconnect function, the COPY command terminates with an error because the MD01 Controller must disconnect from the host adapter before it can select the external device.

NOTE

> The external device must support the **MODE SELECT** command so that the MD01 Controller can determine the block size of a direct-access device (disk drive).

The Initiator is responsible for properly positioning any sequential devices before beginning the COPY command. Any necessary error-recovery procedures for any external device are also the responsibility of the Initiator.

The MD01 Controller may disconnect from the Initiator on the SCSI bus during execution of this command without an error message being generated.

The MD01 Controller supports block sizes of 256 and 512 bytes for external devices.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the device that is to receive the copied data.

Length of Parameter List - Bytes 02 through 04

The COPY command Parameter List specifies the length in bytes of the parameters that are sent during the Data Out Phase of the COPY command. The Parameter List is sent to the MD01 Controller as data with Bytes 02 through 04 of the CDB specifying the length of the Parameter List. A zero value in the length indicates no copy of any data, but this condition is not treated as an error.

The COPY command Parameter List begins with a four-byte header that contains the Copy Function Code. After the header, one or more segment descriptors are provided. The format, length, and number of segment descriptors are determined by the Copy Function Code (see Table 8-1). Up to 256 segment descriptors are permitted. The segment descriptors are identified by ascending numbers, beginning with zero.

Subsequent segments may change the source or destination LUN and device ID, if one of them is internal to the MD01 Controller.

The MD01 Controller supports sequential-to-random access and random-to-random access copy operations (see subsections 8.3.1.1 and 8.3.1.2).

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.1.1 Parameter List Header

The Parameter List begins with a 4-byte header that contains the COPY function code. One or more segment descriptors (see subsection 8.3.1.2) follow the Parameter List header.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	CFC		0	0	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0

Copy Function Code (CFC) - Byte 00, Bits <04:03>

These bits indicate the type of copy operation. Table 8-1 lists and describes the possible Copy Function Codes.

Table 8-1. COPY Command Function Codes

Bits		Description
04	03	
0	0	Random-to-Sequential Access
0	1	Sequential-to-Random Access
1	0	Random-to-Random Access

8.3.1.2 Random-to-Sequential Access and Sequential-to-Random Access Copy Operations

The COPY command segment descriptor for random-to-sequential access and sequential-to-random access copy operations is shown and described below. Up to 256 segment descriptors may be listed, provided they are within the Parameter List Length specified in Bytes 02 through 04 of the COPY CDB.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	SCID			0	0	SLUN		
01	DCID			0	0	DLUN		
02	Sequential Device Block Size in Bytes (MSB)							
03	Sequential Device Block Size in Bytes (LSB)							
04	Number of Blocks (Random Device) (MSB)							
05	Number of Blocks							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	Logical Block Address (Random Device) (MSB)							
09	Logical Block Address							
10	Logical Block Address							
11	Logical Block Address (LSB)							

NOTE

> To perform a random-to-sequential or a sequential-to-random copy operation, the SCSI bus address for the MD01 Controller must be specified in either the Source Controller ID field or the Destination Controller ID field.

Source Controller ID (SCID) - Byte 00, Bits <07:05>

These bits specify the SCSI bus address of the controller for the source device.

Source Logical Unit Number (SLUN) - Byte 00, Bits <02:00>

These bits specify the LUN of the source device.

Destination Controller ID (DCID) - Byte 01, Bits <07:05>

These bits specify the SCSI bus address of the controller for the destination device.

Destination LUN (DLUN) - Byte 01, Bits <02:00>

These bits specify the LUN of the destination device.

Sequential Device Block Size - Bytes 02 and 03

These bytes specify the block size to be used for the sequential access device during the copy operation. If this block size cannot be supported, the MD01 Controller sends a CHECK CONDITION status code to the Initiator and sets the Sense Key in the Extended Sense Byte to the ILLEGAL REQUEST code. During a read or write operation to the sequential access device, if the MD01 Controller determines the block size is invalid, it terminates the copy operation and sends a CHECK CONDITION status code to the Initiator and sets the Sense Key in the Extended Sense Byte to the COPY ABORTED code.

Number of Blocks (Random Device) - Bytes 04 through 07

These bytes specify the number of random access blocks to be transferred in the current segment. A zero value indicates that no blocks are to be transferred in this segment.

Logical Block Address (Random Device) - Bytes 08 through 11

These bytes specify the starting logical block address on the random access device for this Transfer operation.

8.3.1.3 Random-to-Random Access Copy Operations

Up to 256 segment descriptors may be listed provided they are within the Parameter List Length specified in Bytes 02 through 04 of the COPY CDB.

Byte	Bit 07	06	05	04	03	02	01	00
00	SCID			0	0	SLUN		
01	DCID			0	0	DLUN		
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Source Number of Blocks (MSB)							
05	Source Number of Blocks							
06	Source Number of Blocks							
07	Source Number of Blocks (LSB)							
08	Source Logical Block Address (MSB)							
09	Source Logical Block Address							
10	Source Logical Block Address							
11	Source Logical Block Address (LSB)							
12	Destination Logical Block Address (MSB)							
13	Destination Logical Block Address							
14	Destination Logical Block Address							
15	Destination Logical Block Address (LSB)							

Source Controller ID (SCID) - Byte 00, Bits <07:05>

These bits specify the SCSI bus address of the controller for the source device.

Source Logical Unit Number (SLUN) - Byte 00, Bits <02:00>

These bits specify the LUN of the source device.

Destination Controller ID (DCID) - Byte 01, Bits <07:05>

These bits specify the SCSI bus address of the controller for the destination device.

Destination LUN (DLUN) - Byte 01, Bits <02:00>

These bits specify the LUN of the destination device.

Reserved - Bytes 02 through 03

These bytes are reserved and must be zero.

Source Number of Blocks - Bytes 04 through 07

These bytes specify the number of blocks to be transferred to or from the source random access device. A zero value indicates that no blocks are to be transferred in this segment.

Source Logical Block Address - Bytes 08 through 11

These bytes specify the starting Logical Block Address on the source device.

Destination Logical Block Address - Bytes 12 through 15

These bytes specify the starting Logical Block Address on the destination device random-to-random access LUN for this segment of the copy operation.

8.3.1.4 Error and Other Conditions During a Copy Operation

The following paragraphs describe the two classes of unusual conditions that can occur during a copy operation and the ways the MD01 Controller responds to such conditions.

NOTE

Sense data for these unusual conditions must be returned in an Extended Sense Byte format, the Parameter Length field specified in the **REQUEST SENSE** CDB must be 12 hexadecimal.

8.3.1.4.1 Copy Operation Management Errors. The first class consists of those unusual conditions detected by the MD01 Controller when it is managing the data transfer part of the copy operation. The unusual conditions include:

- Invalid parameters in the COPY command
- Invalid segment descriptors

If a copy operation management error occurs, the MD01 Controller performs the following operations:

1) Terminates with CHECK CONDITION status code.
2) Sets the Valid Address (VADD) bit in the Extended Sense Byte to one. Sets the Sense Key to the Sense Key code that describes the unusual condition.
3) Sets Extended Sense Byte 01 to the current Segment Descriptor number. The Segment Descriptors are identified by ascending numbers beginning with zero.
4) Sets the Sense Information Bytes of the Extended Sense Bytes 03 through 06 to the difference (residue) between the value in the Number of Blocks field of the current segment descriptor for the source device and the actual number of source blocks written on the destination device medium.

8.3.1.4.2 Copy Operation Data Transfer Errors. The second class of unusual conditions consists of errors detected by devices on the SCSI bus during the Data Transfer part of the copy operation. The MD01 Controller must recover the Sense data associated with the unusual condition.

After the MD01 Controller recovers the Sense data associated with the detected error, it performs the following operations:

1) Terminates with CHECK CONDITION status code.
2) Sets the VADD bit 07 in Extended Sense Byte 00 to one.
3) Sets the Segment Number in Extended Sense Byte 01 to the number of the current Segment Descriptor being processed at the time the unusual condition is detected. The Segment Descriptors are identified by ascending numbers beginning with zero.
4) Sets the code in the Sense Key field in Extended Sense Byte 02 to the code for COPY ABORTED.

5) Sets the Sense Information Bytes of the Extended Sense Bytes 03 through 06 to the difference (residue) between the value in the Number of Blocks field of the current segment descriptor for the source device and the actual number of source blocks successfully copied.

NOTE

The Additional Sense Length specifies the number of Additional Sense Bytes.

6) Sets the First Additional Sense Length Byte (Byte 08) to the byte number (relative to Byte 00) of the beginning of the source device's Status Byte and Sense data. A zero value in the byte indicates no Status Byte and Sense data are being returned from the source device. If the source device is external to the MD01 Controller, the first byte of the area pointed to by the first Additional Sense Byte contains the completion status from the source device. Subsequent bytes contain the Standard (Non-Extended) Sense data (unchanged) recovered from the source device.

7) Sets the Second Additional Sense Length Byte (Byte 09) to the byte number (relative to Byte 00) of the beginning of the destination device's Status Byte and Sense data. A zero value in this byte indicates no Status Byte and Sense data are being returned from the destination device. If the destination device is external to the MD01 Conroller, the first byte of the area pointed to by the second Additional Sense Byte contains the completion status from the destination device. Subsequent bytes contain the Standard (Non-Extended) Sense data (unchanged) recovered from the destination device.

8.3.2 FORMAT UNIT 04

The **FORMAT UNIT** CDB, shown below, is used to write header and data blocks on the entire disk. All appropriate headers and data sectors are verified and spare sectors/alternate tracks are appropriately re-assigned so that all logical data blocks can be accessed. Defective sector and track files are maintained on the disk by the MD01 Controller on a cylinder that is inaccessible to the Initiator. During the formatting process, sectors with errors and tracks that have more sectors with errors than available spares are re-assigned to spare sectors and alternate tracks, respectively. The Initiator may specify logical blocks to be added to the Bad Sector File.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	0	0
01	LUN			FMD	CPL	Defect List Format		
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Interleave Code (LSB)							
05	0	0	0	0	0	0	Flag	Link

The command in this CDB may disconnect from the Initiator.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Format Data (FMD) - Byte 01, Bit 04

When the FMD bit status is set to one, **FORMAT UNIT** data is supplied during the Data Out Phase of the command. The Defect List, included with this data, specifies the defects to be entered into the Defect Map. The Defect List is formatted in the block format (see subsection 8.3.2.1). When the FMD bit status is reset to zero, the Data Out Phase of the command does not occur and no defect data is supplied by the Initiator.

Complete List (CPL) - Byte 01, Bit 03

When the CPL bit status is set to one, data supplied in the Defect List is the complete list of known defects. Any previous Defect Map or defect data is erased. The Target may add to this Defect List as it formats the media. The CPL bit is set to purge any previously specified Defect List and to build a new Defect List. The MD01 Controller ignores the CPL bit status when it is reset to zero.

Defect List Format - Byte 01, Bits <02:00>

These bits specify additional information related to the format of the Defect List. Together with the FMD and CPL bits, these bits specify the mode of the MD01 Controller during a Format operation. The Format modes are listed in Table 8-2. Only the block address mode is supported.

Interleave Code - Bytes 03 through 04

The code in the Interleave field requests that the logical blocks be related in a specific fashion to the physical blocks to compensate for differences in execution time between the host processor and the MD01 Controller, if necessary. Emulex recommends that a 1:1 sequential interleave be used.

The most significant byte of the Interleave field (Byte 03) must be zero. An Interleave value of zero (hexadecimal) requests that the Target use its default Interleave (1:1 sequential).

If a value greater than 1 is specified in the Interleave field, that number indicates where the next logical block in sequence is located with respect to the logical block just before it. For example, if an interleave code of 3 is specified and n is a logical block, then n+1 is the third contiguous block from n.

Table 8-2. MD01 Controller Format Modes

Bits 04	03	02	01	00	Mode
0	0	0	0	0	Not used.
0	1	0	0	0	**Format Mode.** The MD01 Controller performs a complete format of the specified disk while building a new Bad Sector File. This mode may be used during the Format operation on an uninitialized disk drive.
1	0	0	0	0	Not used.
1	1	0	0	0	**Format Mode with Update.** The MD01 Controller accepts a Defect List from the Initiator which is to be used as the contents of the initial Bad Sector File. Any existing Bad Sector File is lost. If additional defects are found, they are added to the Bad Sector File. This mode may be used to format an uninitialized disk drive by using a zero-length Defect List.

8.3.2.1 Defect List Header

During the Data Out Phase of the **FORMAT UNIT** command, data is sent as a Defect List. The Defect List begins with a 4-byte header which contains the Length of the Defect List (i.e., the total number of bytes sent). One or more defect descriptors (see subsection 8.3.2.2) follow the Defect List header.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
02	Length of Defect List (MSB)							
03	Length of Defect List (LSB)						0	0

Length of Defect List - Bytes 02 through 03

The value in the Length of Defect List field specifies the total number of bytes (not the total number of defect descriptors) sent during the Data Out Phase of the **FORMAT UNIT** command.

8.3.2.2 Format Unit Defect Descriptor Format

The **FORMAT UNIT** defect descriptor is shown below. The total number of defect descriptors sent is dependent on the Defect List Length specified in the **FORMAT UNIT** header (Bytes 02 through 03).

Byte	Bit 07	06	05	04	03	02	01	00
00	Defect List Block Address (MSB)							
01	Defect List Block Address							
02	Defect List Block Address							
03	Defect List Block Address (LSB)							

Defect List Block Address - Bytes 00 through 04

These bytes specify the address of the block that contains the defect.

The Defect List Block Addresses are converted to the appropriate track and block addresses by the MD01 Controller and are specified in ascending order.

8.3.3 INQUIRY 12

The **INQUIRY** CDB, shown below, causes a request to be made for the transfer of data from the Target to the Initiator. The data to be transferred describes unique parameters that are pertinent to the MD01 Controller. The number of bytes transferred depends on the number of bytes requested by the contents of Byte 04. The data transferred includes information about the parameters of the addressed LUN.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	0	1	0
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Number of Bytes in Transfer							
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 03

These bytes are reserved and must be zero.

Number of Bytes in Transfer - Byte 04

This byte specifies the number of bytes the Initiator has allotted for returned **INQUIRY** data. A value of zero indicates no data is transferred. This last situation is not an error condition.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.3.1 Inquiry Data Format

During the Data In Phase of the **INQUIRY** command, data is transferred in the following format:

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	RMD	Device Type Qualifier						
02	0	0	0	0	0	0	REVL	
03	0	0	0	0	0	0	0	0

Byte 00, Bit 00

Byte 00 indicates the Device Type code. Bit 00 is set to zero to indicate that a random-access device is being used with the MD01 Controller.

Removable Media (RMD) - Byte 01, Bit 07

The RMD bit is zero to indicate the media is not removable.

Device Type Qualifier - Byte 01, Bits <06:01>

The bits in this field form a seven-bit user-specified code. The MD01 Controller does not support this feature and returns all zero bits for the Device Type Qualifier field.

Not Used - Byte 02, Bits <07:06>

These bits are not used and can be either one or zero.

Revision Level (REVL) - Byte 02, Bits <01:00>

The REVL bits <01:00> of Byte 02 indicate the revision level of the firmware in the MD01 Controller. If they are set to 00, it is an unspecified revision level; if they are set to 01, it is a first release of the firmware.

8.3.4 MODE SELECT 15

The **MODE SELECT** CDB, shown below, enables an Initiator to specify device parameters to the MD01 Controller.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	0	1
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Parameter List Length							
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 03

These bytes are reserved and must be zero.

Parameter List Length - Byte 04

This byte specifies the length in bytes of the Parameter List sent during the Data Out Phase of this command. The valid hexadecimal value for bits in the Parameter List Length field is 15 for the ST506-compatible disk interface.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.4.1 Mode Select Parameter List

The Mode Select Parameter List, shown below, is sent during the Data Phase of the **MODE SELECT** command to specify parameters for ST506-compatible disk drives.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	VU	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	Block Descriptor Length							
04	0	0	0	0	0	0	0	0
05	Number of Blocks (MSB)							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	0	0	0	0	0	0	0	0
09	Block Length (MSB)							
0A	Block Length							
0B	Block Length (LSB)							
0C	Number of Alternate Cylinders							
0D	Number of Heads				SSZ	SST		BFS
0E	Logical Number of Sectors/Track							
0F	Logical Number of Cylinders (MSB)							
10	Logical Number of Cylinders (LSB)							
11	Write Precompensation Cylinder Number (MSB)							
12	Write Precompensation Cylinder Number (LSB)							
13	Reduced Write Current Cylinder Number (MSB)							
14	Reduced Write Current Cylinder Number (LSB)							

Vendor Unique (VU) - Byte 01

This field is set to 80 (hexadecimal) to specify that Byte 01 is a definition of the Media Type.

Reserved - Byte 02

This byte is reserved and must be zero.

Block Descriptor Length - Byte 03

This byte specifies the length of the Block Descriptor in decimal bytes, starting at Byte 04. Valid lengths are 0 and 17 (decimal).

Density Code - Byte 04

This byte defines the density of the media on the addressed LUN. The Density Code has a value of zero to indicate the LUN is a hard disk drive.

Number of Blocks - Bytes 05 through 07

This field specifies the number of logical blocks in the user's address space. Currently, the MD01 Controller ignores this field.

Reserved - Byte 08

This byte is reserved and must be zero.

Block Length - Bytes 09 through 0B

This field specifies the length of the logical block in bytes. Currently, the MD01 Controller ignores this field.

Number of Alternate Cylinders - Byte 0C

This byte specifies the number of cylinders to be used for alternate addressing. Bad tracks are mapped on the alternate cylinders.

Number of Heads - Byte 0D, Bits <07:04>

These bits specify the number of heads on the disk drive.

Sector Size (SSZ) - Byte 0D, Bit 03

This bit indicates the sector size. If the SSZ bit is set to one, the sector size is 256 bytes. If the SSZ bit is reset to zero, the sector size is 512 bytes.

Spare Sectors/Track (SST) - Byte 0D, Bits <02:01>

These bits indicate the number of spare sectors/track. The bit patterns are listed and described in Table 8-3.

Table 8-3. Spare Sectors/Track Bits

Bits 01	Bits 02	Number of Spare Sectors/Track
0	0	0
0	1	1
1	0	2
1	1	3

Buffered Step (BFS) - Byte 0D, Bit 00

This bit indicates if the disk drive Step operation (involving the time intervals in which the Step signal pulses occur) is or is not to be buffered. If the BFS bit is set to one, the Step operation is buffered. If the BFS bit is reset to zero, the Step operation is non-buffered.

Logical Number of Sectors/Track - Byte 0E

This byte specifies the logical number of sectors per track which can be accessed by the user. The value of this field plus the value of the spare sectors per track field equals the total number of physical sectors per track.

Logical Number of Cylinders - Bytes 0F through 10

The value in this field minus 2 specifies the logical number of cylinders in the user's address space. Two of the cylinders cannot be accessed by the user, because one cylinder is dedicated to the Bad Sector File and the other is dedicated to diagnostic data. The value in this field plus the value of the Number of Alternate Cylinders field equals the total number of physical cylinders.

Write Precompensation Cylinder Number - Bytes 11 through 12

These bytes specify the number of the cylinder at which the disk drive writes data to inner cylinders on the disk using a time-precompensated format. For more information on the Write Precompensation Cylinder Number, see subsection 3.3.1.

Reduced Write Current Cylinder Number - Bytes 13 through 14

These bytes specify the number of the cylinder at which the disk drive supplies a different amount of current to the head during a write operation. For more information on the Reduced Write Current Cylinder Number, see subsection 3.3.1.

8.3.5 MODE SENSE 1A

The **MODE SENSE** CDB, shown below, causes an Initiator to determine the parameters of the MD01 Controller. **MODE SENSE** is a complementary command, related to the **MODE SELECT** command, (see subsection 8.3.4), and is used for support of media that may contain different densities.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Allocation Length							
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 03

These bytes are reserved and must be zero.

Allocation Length - Byte 04

The Allocation Length specifies the number of bytes the Initiator has allocated for returned **MODE SENSE** data. If the MD01 Controller receives a zero value in Byte 04, it does not transfer any data and does not treat this condition as an error. A non-zero Allocation Length value indicates the maximum number of bytes to be transferred. The Target terminates the Data In Phase when the Allocation Length bytes have been transferred or when all available **MODE SENSE** data has been transferred to the Initiator.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.5.1 Mode Sense Data Format

The Mode Sense Parameter List, shown below, is sent during the Data Out Phase of the **MODE SENSE** command to specify parameters for ST506-compatible disk drives.

Byte	Bit 07	06	05	04	03	02	01	00
00	Data Length							
01	VU	0	0	0	0	0	SCT	INTF
02	WRP	0	0	0	0	0	0	0
03	Block Descriptor Length							
04	Density Code							
05	Number of Blocks (MSB)							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	0	0	0	0	0	0	0	0
09	Block Length (MSB)							
0A	Block Length							
0B	Block Length (LSB)							
0C	Number of Alternate Cylinders							
0D	Number of Heads				SSZ	SST		BPS
0E	Logical Number of Sectors/Track							
0F	Logical Number of Cylinders (MSB)							
10	Logical Number of Cylinders (LSB)							
11	Write Precompensation Cylinder Number (MSB)							
12	Write Precompensation Cylinder Number (LSB)							
13	Reduced Write Current Cylinder Number (MSB)							
14	Reduced Write Current Cylinder Number (LSB)							

Data Length - Byte 00

This byte specifies the length of the Parameter List that is returned when a **MODE SENSE** command is issued. Acceptable values for the Parameter List length are 5 and 21. A value of 5 indicates the disk configuration switches are set to invalid (see the description of Block Descriptor Length below). A value of 21 indicates the entire Parameter List will be returned.

Vendor Unique (VU) - Byte 01, Bit 07

This bit is set to one to specify that Byte 01 is a definition of Media Type byte.

Sector Type - Byte 01, Bit 01

This bit indicates the sector type. If the SCT bit is set to one, the LUN supports soft sectoring (i.e., the drive can be formatted with either 256- or 512-byte sectors). If the SCT bit is reset to zero, the LUN supports hard sectoring.

Interface Type (INTF) - Byte 01, Bit 00

This bit indicates the interface type. The INTF bit is always zero to indicate the interface type is ST506-compatible.

Write Protect (WRP) - Byte 02, Bit 07

When the WRP bit is set to one, the disk drive is write protected. When the WRP bit is reset to zero, the disk drive is not write protected.

Block Descriptor Length - Byte 03

This byte specifies the length of the Block Descriptor. Valid lengths are 1 and 17 (decimal). A value of one indicates that the Disk Configuration switches (see subsection 3.3) on the MD01 Controller are set to invalid and a **MODE SELECT** command, which specifies valid Disk Configuration parameters, has not yet been issued to the MD01 Controller. The **MODE SELECT** command must be sent before the MD01 Controller can format the disk drive.

Density Code - Byte 04

This byte defines the density of the media on the addressed LUN. The Density Code has a value of zero to indicate that the LUN is a hard disk drive.

Number of Blocks - Bytes 05 through 07

This field specifies the number of logical blocks in the user's address space.

Block Length - Bytes 09 through 0B

These bytes specify the length of the logical block in bytes.

Number of Alternate Cylinders - Byte 0C

This byte specifies the number of alternate cylinders to be accessed. Bad tracks are mapped on the alternate cylinders.

Number of Heads - Byte 0D, Bits <07:04>

These bits specify the number of heads on the disk drive.

Sector Size (SSZ) - Byte 0D, Bit 03

This bit indicates the sector size (i.e., capacity). If the SSZ bit is set to one, the sector size is 256 bytes. If the SSZ bit is reset to zero, the sector size is 512 bytes.

Spare Sectors/Track (SST) - Byte 0D, Bits <02:01>

These bits indicate the number of spare sectors per track. The bit patterns are listed and described in Table 8-3.

Buffered Step (BFS) - Byte 0D, Bit 00

This bit indicates whether the step is or is not buffered. If the BFS bit is set to one, the step is buffered. If the BFS bit is reset to zero, the step is non-buffered.

Logical Number of Sectors/Track - Byte 0E

This byte specifies the logical number of sectors per track which can be accessed by the user.

Logical Number of Cylinders - Bytes 0F through 10

These bytes specify the logical number of cylinders in the user's address space. Two of the cylinders cannot be accessed by the user because one cylinder is dedicated to the Bad Sector File and the other is dedicated to diagnostic data.

Write Precompensation Cylinder Number - Bytes 11 through 12

These bytes specify the number of the cylinder at which the disk drive writes data to inner cylinders on the disk, using a time-precompensated format. For more information on the Write Precompensation Cylinder Number, see subsection 3.3.1.

Reduced Write Current Cylinder Number - Bytes 13 through 14

These bytes specify the number of the cylinder at which the disk drive supplies a different amount of current to the head during a write operation. The MD01 Controller will supply more current for a write operation on an outer cylinder than on an inner cylinder. For more information on the Reduced Write Current Cylinder Number, see subsection 3.3.1.

8.3.6 READ 08

The **READ** CDB, shown below, causes the transfer of data from the Target device to the Initiator. The **READ** command specifies the starting block number and the number of data blocks to be read. The **READ** command terminates when the number of data blocks to be read is transferred.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	0	1	0	0	0
01	LUN			Logical Block Address (MSB)				
02	Logical Block Address							
03	Logical Block Address (LSB)							
04	Number of Blocks to Transfer (LSB)							
05	ECC	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller can disconnect from the Initiator while executing this command.

If any reservation access conflict exists (see subsection 8.3.11, **RESERVE UNIT** command), the MD01 Controller terminates the **READ** command with a RESERVATION CONFLICT status code; no data is read.

Table 8-4 lists several error conditions, and their corresponding Sense Keys, that can occur during a read operation. If any of the conditions occur, the MD01 Controller terminates the **READ** command, sends a CHECK CONDITION status code to the Initiator, and sets the Sense Key that corresponds to the error condition in the Extended Sense Byte.

Table 8-4. READ Command Error Conditions

Sense Key	Condition
ILLEGAL REQUEST *	An invalid Logical Block Address was issued
UNIT ATTENTION	A Target Reset condition or media change occurred since the last command was sent from this Initiator
MEDIUM ERROR	An unrecoverable Read error occurred
RECOVERED ERROR	A recoverable Read error occurred
ABORTED COMMAND	An error occurred, which might be resolved by repeating the command

* For this Sense Key, the Information Byte is set to the Logical Block Address of the first invalid Logical Block Address. The Logical Block Address is invalid if any part of the extent is invalid.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Logical Block Address - Bytes 01 through 03

These bytes specify the logical block address where the read operation is to begin.

Number of Blocks to Transfer - Byte 04

This byte specifies the number of contiguous logical blocks of data to be transferred. When this byte is zero, 256 logical blocks of data are transferred. Any other value between 1 and 256, inclusive, indicates that number of logical blocks is to be transferred.

Error Correction Code (ECC) - Byte 05, Bit 07

This bit indicates if ECC Checking operations are or are not disabled. If the ECC bit is set to one, ECC Checking operations are disabled. If the ECC bit is reset to zero, ECC Checking operations are enabled.

Error Retry (ERTY) - Byte 05, Bit 06

This bit indicates whether Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Alternate Vectoring (AV) - Byte 05, Bit 05

This bit indicates if Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled, when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.7 RE-ASSIGN BLOCK 07

The RE-ASSIGN BLOCK CDB, shown below, sends Defect List data to the Target during the Data Phase of the command. The defect data is a list of logical block addresses that are to be re-assigned.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	1	1
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

During the Re-assign operation, if all available spares on the track become allocated, the entire track is marked as defective and an alternate track is used. Unspecified data blocks on the track are also moved to the alternate track. The alternate track is fully verified before the original track is marked as defective. If the RE-ASSIGN BLOCK command is completed successfully, no blocks are altered by the command, except those blocks indicated in the Defect List.

If the MD01 Controller is unable to update the defective sector file on the specified disk drive, an error occurs.

If the disconnect function is enabled, the MD01 Controller may disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 04

These bytes are reserved and must be zero.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.7.1 Re-assign Block Header

During the Data Out Phase of the **RE-ASSIGN BLOCK** command, data is sent as a Defect List. The Defect List begins with a 4-byte header that contains the Length of the Defect List (i.e., the total number of bytes sent). One or more defect descriptors (see subsection 8.3.7.2) follow the Defect List header.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
02	Length of Defect List (MSB)							
03	Length of Defect List (LSB)						0	0

Length of Defect List - Bytes 02 through 03

The value in the Length of Defect List field specifies the total number of bytes (not the total number of defect descriptors) sent during the Data Out Phase of the **RE-ASSIGN BLOCK** command.

8.3.7.2 Re-assign Block Defect Descriptor Format

The **RE-ASSIGN BLOCK** defect descriptor is shown below. The total number of defect descriptors sent is dependent on the Defect List Length specified in the **RE-ASSIGN BLOCK** header (Bytes 02 through 03).

Byte	Bit 07	06	05	04	03	02	01	00
00	Defect List Block Address (MSB)							
01	Defect List Block Address							
02	Defect List Block Address							
03	Defect List Block Address (LSB)							

The Defect List Block Address bytes are converted to the appropriate track and block addresses by the MD01 Controller and are specified in ascending order. Block addresses that specify previously detected or specified addresses are processed and produce duplicate entries in the Bad Sector File if the re-assignment results in the use of another spare block.

If the LUN has insufficient capacity to re-assign all the defective logical blocks, the MD01 command terminates the **RE-ASSIGN BLOCK** command with a CHECK CONDITION status code and sets the Sense Key in the Extended Sense Byte to MEDIUM ERROR. The Logical Block Address of the last logical block re-assigned is returned in the Information Bytes of the sense data.

Defect List Block Address - Bytes 00 through 03

These bytes specify the address of the block that contains the defect.

8.3.8 RECEIVE DIAGNOSTIC 1C

The **RECEIVE DIAGNOSTIC** command allows the MD01 Controller to start diagnostic subcommands sent by the **SEND DIAGNOSTIC** command (see subsection 8.3.15). The **RECEIVE DIAGNOSTIC** command is executed only by the MD01 Controller if a **SEND DIAGNOSTIC** command previously was issued by the same Initiator that issued the **RECEIVE DIAGNOSTIC** command. If no **SEND DIAGNOSTIC** command has been received, the MD01 Controller rejects the **RECEIVE DIAGNOSTIC** command with a CHECK CONDITION status code and sets the ILLEGAL REQUEST Sense Key in the Extended Sense Byte (see subsection 8.3.10.2).

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	1	1	1	0	0
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	Allocation Length							
04	Allocation Length							
05	0	0	0	0	0	0	Flag	Link

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device to be loaded or unloaded.

Reserved - Bytes 02

This byte is reserved and must be zero.

Allocation Length - Bytes 03 through 04

These bytes specify the number of bytes the Initiator has allocated for returned diagnostic data. If the Allocation Length has a value of zero, no diagnostic data is returned. If the Allocation Length has any other value, that number of bytes or fewer are transferred. The Target terminates the Data In Phase when all Allocation Length bytes have been transferred, or when all available diagnostic data has been transferred to the Initiator. If the value in this field is different from the default length associated with a particular command, the MD01 Controller uses the value in this Allocation Length field instead of the default value.

NOTE

> Although diagnostic software is generally device-specific, the **RECEIVE DIAGNOSTIC** and **SEND DIAGNOSTIC** commands enable the system to isolate host operating system software from device-specific diagnostic software. This isolation allows the host operating system to remain device independent.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 of Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command for the Initiator. Status is returned for each command executed.

NOTE

> Data returned with the **RECEIVE DIAGNOSTIC** command is transferred in the format shown in the descriptions of the individual diagnostic subcommands associated with the **SEND DIAGNOSTIC** command (see subsection 8.3.14).

8.3.9 RELEASE UNIT 17

The **RELEASE UNIT** CDB, shown below, causes the LUN (connected to the MD01 Controller and previously reserved by the **RESERVE UNIT** command; see subsection 8.3.11) to be released. The LUN is released if the requesting Initiator was the last to reserve that LUN. Once the **RELEASE UNIT** command is issued, other Initiators can access the LUN.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	1	1
01	0	0	0	THPR	Third Party ID			0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

It is not an error to attempt to release to the requesting Initiator any LUN which is not currently reserved.

The MD01 Controller does not disconnect from the Initiator while executing this command.

Third Party Reservation Release Option (THPR) - Byte 01, Bit 04

If this bit is set to one, the MD01 Controller releases the LUN (that was reserved using the Third Party Reservation option with the **REQUEST UNIT** command, see subsection 8.3.11) provided the following conditions are true:

- the same Initiator that reserved the LUN is requesting the release of the LUN.
- the Initiator specifies the same SCSI bus device in the Third Party ID field as was specified for that field in the **RESERVE UNIT** command.

Third Party ID - Byte 01, Bits <03:01>

These bits specify the SCSI bus device ID for which the LUN was reserved.

Reserved - Bytes 02 through 04

These bytes are reserved and must be zero.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.10 REQUEST SENSE 03

The **REQUEST SENSE** CDB, shown below, is used to obtain more detailed information after execution of a command. Typically, a **REQUEST SENSE** command is issued after a previous command has completed and a CHECK CONDITION status code has been issued to the Initiator. The MD01 Controller saves the Sense data for the LUN that was involved in the operation for which a CHECK CONDITION status code was returned.

An Initiator should issue a **REQUEST SENSE** command as soon as it receives a CHECK CONDITION status code to obtain the Sense data saved by the MD01 Controller. The Initiator can issue several **REQUEST SENSE** commands at this time to obtain the Extended Sense Byte data (see subsection 8.3.10.2) as well as the Standard Sense Byte data (see subsection 8.3.10.1). However, when the MD01 Controller receives any other command other than **REQUEST SENSE**, it clears the Sense data.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	1	1
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Number of Requested Sense Bytes							
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 03

These bytes are reserved and must be zero.

Number of Requested Sense Bytes - Byte 04

This byte contains the number of bytes of data the Initiator has allocated for the sense information. The count supplied determines the format of the returned sense data. The sense data can be returned in one of two supported Sense Byte Formats:

- Standard (non-extended)
- Extended

These formats are described in subsections 8.3.10.1 and 8.3.10.2.

A requested sense byte count of four or fewer bytes results in a transfer of four bytes in the Standard Sense Byte format.

A requested sense byte count of more than four bytes results in a data transfer of up to the requested number of sense bytes in the Extended Sense Byte format. The number of bytes transferred never exceeds the maximum number of sense bytes defined.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.10.1 Standard Sense Byte Format

The Standard Sense Byte format, shown below, is used when the requested number of bytes (Byte 04 of the **REQUEST SENSE** CDB) is less than or equal to four.

Byte	Bit 07	06	05	04	03	02	01	00
00	VADD	ERCL			ERCD			
01	0	0	0	Logical Block Address (MSB)				
02	Logical Block Address							
03	Logical Block Address (LSB)							

Valid Address (VADD) - Byte 00, Bit 07

Setting this bit indicates the Logical Block Address field (Bytes 01 through 03) contains valid information related to the error code.

Error Class (ERCL) - Byte 00, Bits <06:04>

These bits indicate the source of the error that occurred. Error Class codes are listed in Table 8-5. Error Classes 0 through 3 (hexadecimal) are valid for Standard Sense information.

Table 8-5. Standard Sense Error Classes

Bits 06 05 04	Error Class
0 0 0	DISK DRIVE ERRORS
0 0 1	TARGET ERRORS
0 1 0	SYSTEM-RELATED ERRORS
0 1 1	VENDOR UNIQUE ERROR CONDITIONS

Error Code (ERCD) - Byte 00, Bits <03:00>

These bits indicate the type of error that occurred. The hexadecimal Sense Codes used in the Standard (nonextended) Sense Bytes for disk drive, Target, and system-related errors are listed and described in Table 8-6.

Logical Block Address - Bytes 01 through 03

These bytes specify the Logical Block Address associated with the Sense Key.

Table 8-6. Standard Sense Error Class/Code Bytes

DISK DRIVE ERRORS		
Hex Code	Error	Description
00	NO SENSE	The MD01 Controller detected no error during execution of the previous command.
02	NO SEEK COMPLETE	The MD01 Controller could not seek to the specified address within an allotted time.
03	WRITE FAULT	The MD01 Controller determined that the Write Fault line (see subsection 6.5) was asserted from the disk drive.
04	DRIVE NOT READY	The disk drive is not ready.
05	DRIVE NOT SELECTED	The drive associated with the specified LUN could not be addressed.
06	NO TRACK ZERO	The MD01 Controller could not rezero the disk drive.
0B	DRIVE TIMEOUT	A timeout occurred during an operation being performed by the disk drive.
TARGET ERRORS		
Hex Code	Error	Description
11	UNCORRECTABLE DATA ERROR	A block could not be written or read after 16 retry attempts.
13	DATA ADDRESS MARK NOT FOUND	An unrecoverable data error occurred during a read operation.

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Table 8-6. Standard Sense Error Class/Code Bytes (continued)

TARGET ERRORS (continued)		
Hex Code	Error	Description
14	BLOCK NOT FOUND	The block sequence is improper, or a block is missing.
15	SEEK ERROR	A miscompare occurred between the cylinder address of the data header and the address specified in the CDB of the command.
16	DMA TIMEOUT ERROR	System activity reached a point where DMA service for the MD01 exceeded allowable time limits and was suspended, requiring one or more retry attempts.
17	WRITE PROTECTED	The disk is write protected. The outstanding **WRITE** command has been aborted.
18	CORRECTABLE DATA CHECK	The MD01 Controller had to read a block two or more times.
19	BAD BLOCK FOUND (VERIFY only)	The MD01 Controller encountered a bad block.
1B	DATA TRANSFER INCOMPLETE	The MD01 could not complete the data transfer operation on the **READ** or **WRITE** command
1D	COMPARE ERROR (VERIFY only)	One or more bytes did not compare when the **VERIFY** command was issued.
1E	CONTROLLER PLL ERROR	The MD01 encountered a phase locked loop (PLL) problem.
1F	RECOVERABLE ERROR	The MD01 retried the operation that caused the recoverable error to occur.

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Table 8-6. Standard Sense Error Class/Code Bytes (continued)

Hex Code	Error	Description
SYSTEM-RELATED ERRORS		
20	INVALID COMMAND	The issued command cannot be executed, or is not applicable.
21	ILLEGAL BLOCK ADDRESS	The addressed block was not within the user's address space.
VENDOR-UNIQUE ERRORS		
30	UNIT ATTENTION	The addressed LUN has been reset. This error is reported the first time any command is issued after the condition is detected; then the requested command is not performed. This condition is cleared when the next command is issued by the same host adapter. UNIT ATTENTION is reported to all SCSI devices that subsequently issue a command to the LUN.
31	COMMAND TIMEOUT	Command execution was not completed by the MD01 Controller before a predetermined, command-specified time limit had expired.
32	NO ALTERNATE TRACKS AVAILABLE	There are no remaining alternate tracks on the addressed LUN. This error condition may occur during the processing of a **FORMAT UNIT** or **RE-ASSIGN BLOCK** command.
35	BAD SECTOR FILE FULL	The Bad Sector File has no remaining space in which to record the entries for the spare block or alternate track assignments.
36	BAD SECTOR FILE INACCESSIBLE	The MD01 Controller could not successfully read from or write to the Bad Sector File.

8.3.10.2 Extended Sense Byte Format

The Extended Sense Byte format, shown below, is used when the requested number of bytes (Byte 04 of the **REQUEST SENSE** CDB) is greater than four.

Byte	Bit 07	06	05	04	03	02	01	00
00	VADD	1	1	1	Vendor Unique Code			
01	Segment Number							
02	X	X	0	0	Sense Key			
03	Logical Block Address (MSB)							
04	Logical Block Address							
05	Logical Block Address							
06	Logical Block Address (LSB)							
07	Additional Sense Length							
08	ERCL				ERCD			

X = Don't Care

Valid Address (VADD) - Byte 00, Bit 07

If this this bit is set, the Logical Block Address (Bytes 03 through 06) contains valid information related to the error code.

Segment Number - Byte 01

This byte contains the current segment number if the Extended Sense information is in response to a COPY command. Up to 256 segments are supported.

Not Used - Byte 02, Bits <07:06>

These bits are not used and can be either one or zero.

Sense Key - Byte 02, Bits <03:00>

The Sense Key bits indicate status information about any errors detected during the operation. The errors are listed and defined in Table 8-7.

Table 8-7. Extended Sense Byte Sense Keys

Hex Code	Error	Description
00	NO SENSE	There is no Sense Key information to be reported for the designated LUN. This code occurs for a successfully completed command.
01	RECOVERED ERROR	The last command was completed successfully, but with some recovery action performed by the Target.
02	NOT READY	The addressed LUN cannot be accessed. Operator intervention may be required.
03	MEDIUM ERROR	The command terminated with a nonrecoverable-error condition which was probably caused by a flaw in the media or by an error in the recorded data.
04	HARDWARE ERROR	A nonrecoverable hardware error (e.g., controller failure, device failure, parity error, etc.) was detected while the Target was performing the command or while the Target was performing a Self-Test operation.

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Table 8-7. Extended Sense Byte Sense Keys (continued)

Hex Code	Error	Description
05	ILLEGAL REQUEST	There was an illegal parameter in the command or in the additional required parameters supplied as data for some related commands.
06	UNIT ATTENTION	The addressed LUN has been reset. This error is reported the first time any command is issued after the condition is detected; then the requested command is not performed. This condition is cleared when the next command is issued by the same host adapter. UNIT ATTENTION is reported to all SCSI devices that subsequently issue a command to the LUN.
07	DATA PROTECT	A write operation was attempted on a write-protected device.
08	RESERVED	
09	VENDOR UNIQUE	A Vendor-Unique error condition occurred. The corresponding nonextended error class and code are specified in Byte 08 of the Extended Sense Byte (see subsection 8.3.10.3).
0A	COPY ABORTED	A COPY command was aborted because an error condition was detected on the source or destination device.

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Table 8-7. Extended Sense Byte Sense Keys (continued)

Hex Code	Error	Description
0B	ABORTED COMMAND	The Target aborted the command. The Initiator may recover by trying to execute the command again.
0C	EQUAL	A **SEARCH DATA** command satisfied an equal comparison.
0D	RESERVED	
0E	MISCOMPARE	Used by the **VERIFY** command to indicate the source data did not match the data read from the disk.
0F	RESERVED	

Logical Block Address - Bytes 03 through 06

These bytes specify the Logical Block Address where the error specified by the Sense Key Error Code occurred.

Additional Sense Length - Byte 07

This byte specifies the number of Additional Sense Bytes that are to follow. If the Allocation Length of the CDB is too small to transfer all of the Additional Sense Length bytes, the Additional Sense Length is not adjusted to reflect the truncation. The Additional Sense Bytes contain command-specific data that further defines the nature of the CHECK CONDITION status code. The Additional Sense Length byte is set to one for all commands except the **COPY** and **SEARCH** commands.

Error Class (ERCL) - Byte 08, Bits <07:04>

The Error Class bits indicate the source of the error that occurred (see Table 8-4). Error Classes 0 through 3 (hexadecimal) are valid for the Extended Sense Information.

Error Code (ERCD) - Byte 08, Bits <03:00>

The Error Code bits indicate the type of error that occurred. The hexadecimal Sense Error Codes used in the Extended Sense Byte for the tape drive, Target, and system-related errors are listed and described in Table 8-5.

General media-related and drive-related error conditions that occur during MD01 Controller disk operations are listed and described in Appendix A.

8.3.11 RESERVE UNIT 16

The **RESERVE UNIT** CDB, shown below, causes the LUN to be reserved for exclusive use by the Initiator until that Initiator sends an appropriate **RELEASE UNIT** command (see subsection 8.3.9). When the MD01 Controller is reserved by an Initiator, if another Initiator issues a command to the MD01 Controller, the MD01 Controller sends a RESERVATION CONFLICT status code to the other Initiator and disconnects from it.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	1	0
01	LUN			THP	Third Party ID			0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The LUN retains the reservation until it is released by the same Initiator that reserved it. Any attempt by another Initiator to obtain the LUN is ignored. The MD01 Controller does not disconnect from the SCSI bus during execution of this command.

Third Party Reservation Option (THP) - Byte 01, Bit 04

This bit allows an Initiator to reserve a LUN for another device on the SCSI bus. If the THP bit is set, an Initiator is allowed to reserve the specified LUN for the SCSI bus device specified in the Third Party ID field (Byte 01, Bits <03:00>). This option is intended for use in multiple-host adapter systems in which the COPY command is used. Any Target that uses the THP option must also use the Third Party Reservation Release (THPR) option (see subsection 8.3.9).

Third Party ID - Byte 01, Bits <03:01>

These bits specify the SCSI bus device ID that identifies the device for which the MD01 Controller is being returned. The ID is valid only when the THP bit (Byte 01, Bit 04) is set.

Reserved - Bytes 03 through 04

These bytes are reserved and must be zero.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.12 REZERO UNIT 01

The **REZERO UNIT** CDB, shown below, causes the selected disk drive to perform a recalibration of the head mechanism to physical cylinder 0.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	1
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	ERTY	0	0	0	0	Flag	Link

The MD01 Controller can disconnect during the execution of this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Byte 04

This byte is reserved and must be zero.

Error Retry (ERTY) - Byte 05, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.13 SEEK 0B

The SEEK CDB, shown below, causes the selected disk drive to begin a Seek operation to the specified logical block location. If the logical block number specifies a block on a defective track, the Seek operation to the alternate track is not performed until the MD01 Controller receives and processes an I/O command.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	1	0	1	1
01	LUN			Logical Block Address (MSB)				
02	Logical Block Address							
03	Logical Block Address (LSB)							
04	0	0	0	0	0	0	0	0
05	0	ERTY	0	0	0	0	Flag	Link

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Logical Block Address - Bytes 01 through 03

These bytes specify the logical block where the Seek operation is to begin.

Reserved - Byte 04

This byte is reserved and must be zero.

Error Retry (ERTY) - Byte 05, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.14 SEND DIAGNOSTIC 1D

The **SEND DIAGNOSTIC CDB**, shown below, causes a diagnostic subcommand to be sent to the Target. The subcommand is specified in the Parameter List of the CDB. The subcommands currently supported by the MD01 Controller are listed in the subsections that follow the explanation of the **SEND DIAGNOSTIC CDB**.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	1	0	1
01	LUN			0	0	ST	0	0
02	0	0	0	0	0	0	0	0
03	Parameter List Length (MSB)							
04	Parameter List Length (LSB)							
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Self-Test - Byte 01, Bit 02

If this bit is set, the Target is directed to complete its default Self-Test procedure. This action automatically resets the MD01 Controller. The host adapter must then resubmit any previously submitted device parameters to the MD01 Controller.

Reserved - Byte 02

This byte is reserved and must be zero.

Parameter List Length - Bytes 03 through 04

These bytes specify the length (in bytes) of the Parameter List transferred during the Data Out Phase of the **SEND DIAGNOSTIC** command. The Parameter List contains a diagnostic subcommand and any additional information required.

The subcommand specified in the Parameter List is executed when the MD01 Controller receives a **RECEIVE DIAGNOSTIC** (see subsection 8.3.8) command from the same Initiator that issued the **SEND DIAGNOSTIC** command.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.14.1 PERFORM DRIVE DIAGNOSTICS 02

The **PERFORM DRIVE DIAGNOSTICS** diagnostic subcommand, shown below, causes the MD01 Controller to perform Write and Verify operations on each surface of the diagnostic cylinder of the specified disk drive. If any sectors on this cylinder cannot be written or verified by using two different bit patterns, the MD01 Controller terminates the command with a CHECK CONDITION status code. The MD01 Controller then sets the Sense Key in the Extended Sense Byte to MEDIA ERROR and sets the Valid Address bit in the Extended Sense Byte to one. The Sense Information bytes contain the number of bad sectors found on this cylinder.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0

Subcommand Code - Byte 00

This byte is set to 02 (hexadecimal) to specify the **PERFORM DRIVE DIAGNOSTICS** diagnostic subcommand.

Reserved - Bytes 01 through 05

These bytes are reserved and must be zero.

8.3.14.2 READ BAD SECTOR FILE 05

The **READ BAD SECTOR FILE** diagnostic subcommand, shown below, causes the MD01 Controller to transfer the contents of the Bad Sector File to the Initiator. During the Transfer operation, the Bad Sector File header is the first information transferred followed by up to the maximum number of entries requested by the Initiator. If fewer than the requested number of entries exist, after all existing entries have been transferred, an error occurs. In this situation, the MD01 Controller sets the Sense Key in the Extended Sense Byte to ILLEGAL REQUEST and sets the Additional Sense Bytes to the Residue Entry Count.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	0	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Requested Entry Count (M) (MSB)							
05	Requested Entry Count (M) (LSB)							

The MD01 Controller begins to execute the subcommand and transfer data when it has received the appropriate **RECEIVE DIAGNOSTIC** command from the Initiator. For information about the data and header format, see subsection 5.3.1.

Subcommand Code - Byte 00

This byte is set to 05 (hexadecimal) to specify the **READ BAD SECTOR FILE** diagnostic subcommand.

Reserved - Bytes 01 through 03

These bytes are reserved and must be zero.

Requested Entry Count - Bytes 04 through 05

These bytes specify the number of entries in the Bad Sector File requested by the Initiator.

8.3.14.3 READ DISK PARTITIONS 06

The **READ DISK PARTITIONS** diagnostic subcommand, shown below, causes the MD01 Controller to return the block addresses of the bad sector file, alternate track area, and diagnostic area.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0

The MD01 Controller begins to execute the subcommand and transfer data when it has received the appropriate **RECEIVE DIAGNOSTIC** command from the Initiator. For information about the data format, see subsection 8.3.14.3.1.

Subcommand Code - Byte 00

This byte is set to hexadecimal 06 to specify the **READ DISK PARTITIONS** diagnostic subcommand.

Reserved - Bytes 01 through 05

These bytes are reserved and must be zero.

8.3.14.3.1 READ DISK PARTITIONS Data Format. Data for the **READ DISK PARTITIONS** diagnostic subcommand is transferred in the following format:

	Bit							
Byte	07	06	05	04	03	02	01	00
(Start of Bad Sector File)								
00	PHAD	Block Address (MSB)						
01	Block Address							
02	Block Address							
03	Block Address (LSB)							
(Start of Alternate Track Storage)								
04	Logical Block Address (MSB)							
05	Logical Block Address							
06	Logical Block Address							
07	Logical Block Address (LSB)							
(Start of Diagnostic Cylinder)								
08	Logical Block Address (MSB)							
09	Logical Block Address							
0A	Logical Block Address							
0B	Logical Block Address (LSB)							

PHAD - Byte 01, Bit 07

This bit indicates if the MD01 Controller interprets the address (specified in Bytes 0 through 3) as a physical address or as a logical address. The PHAD bit is always set to one to indicate the MD01 Controller interprets the address as a physical address.

Bad Sector File Physical Block Address - Bytes 00 through 03

These bytes specify the starting block address of the Bad Sector File. Note that the PHAD bit is always set to

Alternate Track Storage Logical Block Address - Bytes 04 through 07

These bytes specify the starting logical block address of the Alternate Track Storage.

Diagnostic Cylinder Logical Block Address - Bytes 08 through 0B

These bytes specify the starting logical block address of the Diagnostic Cylinder.

8.3.14.4 READ LONG 1A

The **READ LONG** diagnostic subcommand, shown below, causes the MD01 Controller to perform a read operation of one data block, beginning at the specified block address. The data and the six Error Correction Code (ECC) bytes of the specified block are transferred to the Initiator. The ECC bytes follow the data.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	PHAD	Block Address (MSB)						
02	Block Address							
03	Block Address							
04	Block Address (LSB)							
05	0	0	0	0	0	0	0	0

The MD01 Controller begins to execute and transfer data when it has received the appropriate **RECEIVE DIAGNOSTIC** command from the Initiator.

Subcommand Code - Byte 00

This byte is set to hexadecimal 1A to specify the **READ LONG** diagnostic subcommand.

PHAD - Byte 01, Bit 07

This bit indicates if the MD01 Controller interprets the address (specified in Bytes 2 through 5) as a physical address or as a logical address. If the PHAD bit is set to one, the MD01 Controller interprets the address as a physical address. If the PHAD bit is zero, the MD01 Controller interprets the address as a logical address.

Block Address - Bytes 01 through 04

These bytes specify the block address where the Read Long Diagnostic operation is to begin.

Reserved - Byte 05

This byte is reserved and must be zero.

8.3.14.5 WRITE LONG 1B

The **WRITE LONG** diagnostic subcommand, shown below, causes the MD01 Controller to perform a write operation of one data block, starting at the specified logical block address. The data and the six ECC bytes of the specified logical block are written for each logical block specified in the logical block address. It is assumed that the ECC bytes follow the data.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	1
01	PHAD	Block Address (MSB)						
02	Block Address							
03	Block Address							
04	Block Address (LSB)							
05	0	0	0	0	0	0	0	0

Subcommand Code - Byte 00

This byte is set to hexadecimal 1B to specify the **WRITE LONG** diagnostic subcommand.

PHAD - Byte 01, Bit 07

This bit indicates if the MD01 Controller interprets the address (specified in Bytes 2 through 5) as a physical address or as a logical address. If the PHAD bit is set to one, the MD01 Controller interprets the address as a physical address. If the PHAD bit is zero, the MD01 Controller interprets the address as a logical address.

Block Address - Bytes 01 through 04

These bytes specify the block address where the Write Long Diagnostic operation is to begin.

Reserved - Byte 05

This byte is reserved and must be zero.

8.3.15 TEST UNIT READY 00

The **TEST UNIT READY** CDB, shown below, causes a test to be performed to ensure the disk drive is powered-on and ready. This condition is indicated by a GOOD status code being returned in response to this command. The MD01 Controller can also return a CHECK CONDITION or BUSY status code in response to this command. If the disk drive is not ready, a **REQUEST SENSE** command can be issued to obtain detailed information about the reason the disk drive is not ready (unavailable).

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect during execution of this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 04

These bytes are reserved and must be zero.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.16 WRITE 0A

The **WRITE** CDB, shown below, causes data to be transferred from the Initiator to the Target device. The amount of data written is a multiple of the block length. The **WRITE** command specifies the starting logical block number and the number of blocks to be written.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	1	0	1	0
01	LUN			Logical Block Address (MSB)				
02	Logical Block Address							
03	Logical Block Address (LSB)							
04	Number of Blocks in Transfer							
05	0	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller may disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Logical Block Address - Bytes 01 through 03

These bytes specify the logical block where the write operation is to begin.

Number of Blocks to Transfer - Byte 04

This byte specifies the number of contiguous logical blocks of data to be transferred. When this byte contains all zeros, 256 logical blocks of data are transferred. Any other Number of Blocks to Transfer value indicates that number of blocks are to be transferred.

Error Retry (ERTY) - Byte 05, Bit 06

This bit indicates whether Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Alternate Vectoring (AV) - Byte 05, Bit 05

This bit indicates whether Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled and when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4 SCSI GROUP CODE 1 COMMAND DESCRIPTIONS

SCSI Group Code 1 command names and operation codes supported by the MD01 Controller are listed by subsection number in the following table:

Subsection	MD01 Controller SCSI Command	Code
8.4.1	**READ CAPACITY**	25
8.4.2	**READ (EXTENDED)**	28
8.4.3	**SEARCH DATA EQUAL**	31
8.4.4	**SEARCH DATA HIGH**	30
8.4.5	**SEARCH DATA LOW**	32
8.4.6	**SEEK (EXTENDED)**	2B
8.4.7	**VERIFY**	2F
8.4.8	**WRITE (EXTENDED)**	2A
8.4.9	**WRITE AND VERIFY**	2E

This subsection provides detailed descriptions of the commands, including CDB formats, hexadecimal operation code, byte and bit functions, and any necessary effects produced by the commands. Each MD01 Controller SCSI command is described in a separate subsection.

A sample Group 1 CDB is shown in Figure 8-2. The first byte of a command (Byte 00) contains two fields: the Group Code in the high-order three bits (bits <07:05>), and the Command Code in the low-order five bits (bits <04:00>). The Group Code determines the length of the command packet in the CDB, and together the Group and Command Codes determine the operation to be performed.

Bits <07:05> of byte 01 in the CDB contain the LUN of the device being addressed. The MD01 Controller, acting as a SCSI Target, supports up to two LUNs (ST506-compatible disk drives). Therefore, the value for the LUN field in byte 01 in the CDB is either 000 or 001. The LUN must be specified for all commands. If a LUN value, issued by the Initiator in an IDENTIFY message, differs from the value specified in the CDB, that value supersedes the value specified in the CDB. The definition of the low-order bits in byte 01 is based on the current command.

The last byte (byte 09) in every CDB is a Control Byte which is differentiated into two groups:

- The low-order two bits control the ability to link commands in a sequence and to notify the host adapter that a particular command (CDB) step has been completed. These two bits are designated Flag and Link in the descriptions of command packets presented in this subsection for the MD01 Controller.
- The remaining bits in the Control Byte indicate whether the Error Retry, ECC Checking, and Alternate Vectoring operations are or are not disabled.

The remaining bytes in the CDB contain Command-Dependent Parameters.

NOTE

> If a byte in a CDB can be any bit pattern, it is specified as Not Used in the paragraphs describing that CDB. If a byte in a CDB must be all zeros, it is specified as Reserved in the paragraphs describing that CDB.

Byte	Bit 07	06	05	04	03	02	01	00
00	Group Code			Command Code				
01	LUN			Command-Dependent Parameters				
02	Command-Dependent Parameters							
03	Command-Dependent Parameters							
04	Command-Dependent Parameters							
05	Command-Dependent Parameters							
06	Command-Dependent Parameters							
07	Command-Dependent Parameters							
08	Command-Dependent Parameters							
09	0	0	0	0	0	0	Flag	Link

Figure 8-2. Sample Group 1 Command Descriptor Block

8.4.1 READ CAPACITY 25

The **READ CAPACITY** CDB, shown below, is used to determine the maximum logical block number on the specified LUN which can be read from or written to by the Initiator, and to determine the size of a logical block.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	1	0	0	1	0	1
01	LUN			0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0
06	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0
08	0	0	0	0	0	0	0	0
09	0	0	0	0	0	0	Flag	Link

The MD01 Controller does not disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Reserved - Bytes 02 through 08

These bytes are reserved and must be zero.

NOTE

The MD01 Controller does not support the Partial Medium Indicator (PMI) bit described in the ANSI SCSI Specification; therefore, Bytes 02 through 08 of the **READ CAPACITY** CDB are reserved and must be equal to zero.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4.1.1 Read Capacity Data Format

During the Data In Phase of the **READ CAPACITY** command, data is sent in the following format:

	Bit							
Byte	07	06	05	04	03	02	01	00
00	Last Block Address (MSB)							
01	Last Block Address							
02	Last Block Address							
03	Last Block Address (LSB)							
04	Block Size (MSB)							
05	Block Size							
06	Block Size							
07	Block Size (LSB)							

Last Block Address - Bytes 00 through 03

These bytes specify the logical block address of the last logical block of the LUN. These bytes exclude the bad sector file, the alternate track area, and the diagnostic area.

Block Size (in Bytes) - Bytes 04 through 07

These bytes specify (in bytes) the number of bytes in the logical block. The Most Significant Byte (MSB) of the Block Size is Byte 04; however, the Block Size is limited to 256 or 512 bytes only.

8.4.2 READ (EXTENDED) 28

The **READ (EXTENDED)** CDB, shown below, performs the same function as the Group 0 **READ** command (see subsection 8.3.6): it causes the transfer of data from the Target device to the Initiator. The amount of transferred data is a multiple of the block length (i.e., 512 data bytes/block). The **READ (EXTENDED)** command specifies the starting block number and the number of data blocks to be read. The **READ (EXTENDED)** command terminates when the number of data blocks to be read has been transferred.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	1	0	1	0	0	0
01	LUN			0	0	0	0	RELA
02	Logical Block Address (MSB)							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	Number of Blocks (MSB)							
08	Number of Blocks (LSB)							
09	ECC	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller can disconnect from the Initiator while executing this command.

If any reservation access conflict exists (see subsection 8.3.11, **RESERVE UNIT** command), the MD01 Controller terminates the **READ (EXTENDED)** command with a RESERVATION CONFLICT status code; no data is read.

Table 8-3 (see subsection 8.3.6) lists several error conditions, and their corresponding Sense Keys, that can occur during a read operation. If any of the conditions occur, the MD01 Controller terminates the **READ (EXTENDED)** command, sends a CHECK CONDITION status code to the Initiator, and sets the Sense Key that defines the error condition in the Extended Sense Byte.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Relative Address (RELA) - Byte 01, Bit 00

Setting this bit to one causes the Logical Block Address to be treated as a two's complement displacement. This displacement is added to the Logical Block Address last accessed on the LUN to form the Logical Block Address for this command. This feature is only available when the linking commands function is performed. The feature requires a previous command in the linked group to have accessed a Logical Block on the LUN; if it has not, the MD01 Controller terminates the **READ (EXTENDED)** command, sends a CHECK CONDITION status code, and sets the Sense Key in the Extended Sense Byte to the ILLEGAL REQUEST code.

Logical Block Address - Bytes 02 through 05

These bytes specify the logical block address where the Extended read operation is to begin.

Reserved - Byte 06

This byte is reserved and must be zero.

Number of Blocks - Bytes 07 through 08

This byte specifies the number of contiguous logical blocks of data to be transferred. When this byte contains all zeros, no logical blocks of data are transferred. Any other value between 1 and 256, inclusive, indicates that number of logical blocks are to be transferred.

Error Correction Code (ECC) - Byte 09, Bit 07

This bit indicates if ECC Checking operations are or are not disabled. If the ECC bit is set to one, ECC Checking operations are disabled. If the ECC bit is reset to zero, ECC Checking operations are enabled.

Error Retry (ERTY) - Byte 09, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Alternate Vectoring (AV) - Byte 09, Bit 05

This bit indicates if Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled, when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

SCSI Group Code 1 Command Descriptions

8.4.6 SEEK (EXTENDED) 2B

The **SEEK (EXTENDED)** CDB, shown below, causes the selected disk drive to begin a Seek operation to the specified logical block location. If the logical block number specifies a block on a defective track, the Seek operation to the alternate track is not performed until the MD01 Controller receives and processes an I/O command.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	1	0	1	0	1	1
01	LUN			0	0	0	0	0
02	Logical Block Address (MSB)							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0
08	0	0	0	0	0	0	0	0
09	0	ERTY	0	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller can disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Logical Block Address - Bytes 02 through 05

These bytes specify the logical block where the Extended Seek operation is to begin.

Reserved - Bytes 06 through 08

These bytes are reserved and must be zero.

Error Retry (ERTY) - Byte 09, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 09) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4.7 VERIFY 2F

The **VERIFY** CDB, shown below, causes the specified number of blocks to be verified.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	1	0	1	1	1	1
01	LUN			0	0	0	BYTC	RELA
02	Logical Block Address (MSB)							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	Number of Blocks (MSB)							
08	Number of Blocks (LSB)							
09	ECC	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller can disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Byte Check (BYTC) - Byte 01, Bit 01

Setting this bit to one causes the specified logical blocks to be read and compared with the data in the data buffer. Data is transferred from the Initiator just as in a write operation. If the BYTC bit is reset to zero, the data is just read and and the ECC is checked for correctness; no Data Transfer operation occurs between the Initiator and the Target.

Relative Address (RELA) - Byte 01, Bit 00

Setting this bit to one causes the Logical Block Address to be treated as a two's complement displacement. This displacement is added to the Logical Block Address last accessed on the LUN to form the Logical Block Address for this command. This feature is only available when the linking command function is performed. The feature requires that a previous command in the linked group has accessed a Logical Block on the LUN; if it has not, the MD01 Controller terminates the **VERIFY** command, sends a CHECK CONDITION status code, and sets the Sense Key in the Extended Sense Byte to the ILLEGAL REQUEST code.

Logical Block Address - Bytes 02 through 05

These bytes specify the logical block where the Verify operation is to begin.

Reserved - Byte 06

This byte is reserved and must be zero.

Number of Blocks - Bytes 07 through 08

This byte specifies the number of contiguous logical blocks of data to be verified. When the Number of Blocks to Transfer is zero, no logical blocks of data are verified. Any other value between 1 and 256, inclusive, indicates that number of logical blocks are to be verified.

Error Retry (ERTY) - Byte 09, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Error Correction Code (ECC) - Byte 09, Bit 07

This bit indicates if ECC Checking operations are or are not disabled. If the ECC bit is set to one, ECC Checking operations are disabled. If the ECC bit is reset to zero, ECC Checking operations are enabled.

Alternate Vectoring (AV) - Byte 09, Bit 05

This bit indicates if Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled, when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 09) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4.8 WRITE (EXTENDED) 2A

The **WRITE (EXTENDED)** CDB, shown below, performs the same function as the Group 0 **WRITE** command (see subsection 8.13.16); it causes data to be transferred from the Initiator to the Target device. The amount of data written is a multiple of the block length. The **WRITE (EXTENDED)** command specifies the starting logical block number and the number of blocks to be written.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	1	0	1	0	1	0
01	LUN			0	0	0	0	RELA
02	Logical Block Address (MSB)							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	Number of Blocks (MSB)							
08	Number of Blocks (MSB)							
09	ECC	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller may disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Logical Block Address - Bytes 02 through 05

These bytes specify the logical block where the Extended write operation is to begin.

Reserved - Byte 06

This byte is reserved and must be zero.

Number of Blocks - Bytes 07 through 08

This byte specifies the number of contiguous logical blocks of data to be transferred. When the Number of Blocks to Transfer is zero, no logical blocks of data are transferred. Any other value between 1 and 256, inclusive, indicates that number of logical blocks are to be transferred.

Error Correction Code (ECC) - Byte 09, Bit 07

This bit indicates if ECC Checking operations are or are not disabled. If the ECC bit is set to one, ECC Checking operations are disabled. If the ECC bit is reset to zero, ECC Checking operations are enabled.

Error Retry (ERTY) - Byte 09, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Alternate Vectoring (AV) - Byte 09, Bit 05

This bit indicates if Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled, when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4.9 WRITE AND VERIFY 2E

The **WRITE AND VERIFY** CDB, shown below, causes data for the specified number of blocks to be written and then verified.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	0	0	1	0	1	1	1	0
01	LUN			0	0	0	BYTC	RELA
02	Logical Block Address (MSB)							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	Number of Blocks (MSB)							
08	Number of Blocks (LSB)							
09	0	ERTY	AV	0	0	0	Flag	Link

If the disconnect function is enabled, the MD01 Controller may disconnect from the Initiator while executing this command.

Logical Unit Number (LUN) - Byte 01, Bits <07:05>

These bits specify the LUN of the addressed device for this command.

Byte Check (BYTC) - Byte 01, Bit 01

Setting this bit to one causes the specified logical blocks to be read and compared with the data sent from the Initiator the second time for the verify operation. Data is transferred from the Initiator just as in a write operation. If the BYTC bit is zero, the data is just read and and the ECC is checked for correctness; no Data Transfer operation occurs between the Initiator and the Target.

Relative Address (RELA) - Byte 01, Bit 00

Setting this bit to one causes the Logical Block Address is treated as a two's complement displacement. This displacement is added to the Logical Block Address last accessed on the LUN to form the Logical Block Address for this command. This feature is only available when the linking command function is performed. The feature requires that a previous command in the linked group has accessed a Logical Block on the LUN; if it has not, the MD01 Controller terminates the **WRITE AND VERIFY** command, sends a CHECK CONDITION status code, and sets the Sense Key in the Extended Sense Byte to the ILLEGAL REQUEST code.

Logical Block Address - Bytes 02 through 05

These bytes specify the logical block where the Write and Verify operation is to begin.

Reserved - Byte 06

This byte is reserved and must be zero.

Number of Blocks - Bytes 07 through 08

This byte specifies the number of contiguous logical blocks of data to be transferred. When the Number of Blocks to Transfer is zero, no logical blocks of data are transferred. Any other value between 1 and 256, inclusive, indicates that number of logical blocks are to be transferred.

Error Retry (ERTY) - Byte 09, Bit 06

This bit indicates if Error Retry operations are or are not disabled. If the ERTY bit is set to one, Error Retry operations are disabled. If the ERTY bit is reset to zero, Error Retry operations are enabled.

Alternate Vectoring (AV) - Byte 09, Bit 05

This bit indicates if Alternate Vectoring operations are or are not enabled. When Alternate Vectoring operations are enabled, when the MD01 Controller performs a Seek operation to a command-specified sector that is on a defective track, it causes the disk drive to perform a Seek operation to the alternate track that contains the valid sector.

If the AV bit is set to one, Alternate Vectoring operations are disabled. If the AV bit is reset to zero, Alternate Vectoring operations are enabled.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 09) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.5 SCSI GROUP CODE 6 COMMAND DESCRIPTIONS

SCSI Group code 6 commands are vendor-unique SCSI commands. Group code 6 command names and operation codes supported by the MD01 Controller are listed by subsection number in the following table:

Subsection	MD01 SCSI Command	Code
8.5.1	**READ LONG**	E8
8.5.2	**WRITE LONG**	EA

This subsection provides detailed descriptions of the commands, including CDB formats, hexadecimal operation code, byte and bit functions, and any necessary event-sequence descriptions (i.e., effects produced by the commands). Each MD01 Controller SCSI command is described in a separate subsection.

A sample Group 6 CDB is shown in Figure 8-3. The first byte of a command (Byte 00) contains two fields: the Group Code in the high-order three bits (bits <07:05>), and the Command Code in the low-order five bits (bits <04:00>). The Group Code determines the length of the command packet in the CDB, and together the Group and Command Codes determine the operation to be performed.

Bits <07:05> of byte 01 in the CDB contain the LUN of the device being addressed. The MD01 Controller, acting as a SCSI Target, supports up to two LUNs (ST506-compatible disk drives). Therefore, the value for the LUN field in byte 01 in the CDB is either 000 or 001. The LUN must be specified for all commands. If a LUN value, issued by the Initiator in an IDENTIFY message, differs from the value specified in the CDB, that value supersedes the value specified in the CDB. The definition of the low-order bits in byte 01 is based on the current command.

The last byte (byte 09) in every CDB is a Control Byte which is differentiated into two groups:

- The low-order two bits control the ability of linking commands in a sequence and of notifying the host adapter that a particular command (CDB) step has been completed. These two bits are designated Flag and Link in the descriptions of command packets presented in this subsection for the MD01 Controller.
- The remaining bits in the Control Byte are reserved bits and are always zero.

The remaining of the bytes in the CDB contain Command-Dependent Parameters.

NOTE

If a byte in a CDB can be any bit pattern, it is specified as **Not Used** in the paragraphs describing that CDB. If a byte in a CDB must be all zeros, it is specified as **Reserved** in the paragraphs describing that CDB.

Byte	Bit							
	07	06	05	04	03	02	01	00
00	Group Code			Command Code				
01	LUN			Command-Dependent Parameters				
02	Command-Dependent Parameters							
03	Command-Dependent Parameters							
04	Command-Dependent Parameters							
05	Command-Dependent Parameters							
06	Command-Dependent Parameters							
07	Command-Dependent Parameters							
08	Command-Dependent Parameters							
09	0	0	0	0	0	0	FLAG	LINK

Figure 8-3. Sample Command Descriptor Block

8.5.1 READ LONG E8

The **READ LONG** command, shown below, causes the MD01 Controller to perform a read operation of one data block, beginning at the specified block address. The data and the six Error Correction Code (ECC) bytes of the specified block are transferred to the Initiator. The ECC bytes follow the data.

Byte	Bit 07	06	05	04	03	02	01	00
00	1	1	1	0	1	0	0	0
01	LUN			0	0	0	0	0
02	PHAD	Block Address (MSB)						
03	Block Address							
04	Block Address							
05	Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0
08	0	0	0	0	0	0	0	0
09	0	0	0	0	0	0	FLAG	LINK

PHAD - Byte 02, Bit 07

This bit indicates if the MD01 Controller interprets the address (specified in Bytes 2 through 5) as a physical address or as a logical address. If the PHAD bit is set to one, the MD01 Controller interprets the address as a physical address. If the PHAD bit is zero, the MD01 Controller interprets the address as a logical address.

Block Address - Bytes 02 through 05

These bytes specify the block address where the read long operation is to begin.

Reserved - Bytes 06 through 08

These bytes are reserved and must be zero.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 09) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.5.2 WRITE LONG EA

The **WRITE LONG** shown below, causes the MD01 Controller to perform a write operation of one data block, starting at the specified logical block address. The data and the six ECC bytes of the specified logical block are written for each logical block specified in the logical block address. It is assumed the ECC bytes follow the data.

Byte	Bit 07	06	05	04	03	02	01	00
00	1	1	1	0	1	0	0	1
01	LUN			0	0	0	0	0
02	PHAD	Block Address (MSB)						
03	Block Address							
04	Block Address							
05	Block Address (LSB)							
06	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0
08	0	0	0	0	0	0	0	0
09	0	0	0	0	0	0	FLAG	LINK

PHAD - Byte 02, Bit 07

This bit indicates if the MD01 Controller interprets the address (specified in Bytes 2 through 5) as a physical address or as a logical address. If the PHAD bit is set to one, the MD01 Controller interprets the address as a physical address. If the PHAD bit is zero, the MD01 Controller interprets the address as a logical address.

Block Address - Bytes 02 through 05

These bytes specify the block address where the write long operation is to begin.

Reserved - Bytes 06 through 08

These bytes are reserved and must be zero.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 09) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

A.1 INTRODUCTION

During MD01 Controller disk operations, when general media-related and drive-related error conditions occur, the MD01 Controller returns a CHECK CONDITION status code to the Initiator. Usually the Initator will then issue a **REQUEST SENSE** command to obtain the Standard Sense codes that describe the error condition. Table A-1 lists Standard Sense keys and their related Standard Sense class and codes. Table A-1 also lists SCSI commands applicable to the Standard Sense key.

Table A-1. General Error Conditions

Sense Key	Sense Code	Applicable Command
NO SENSE (00)	NO SENSE (00)	All commands
RECOVERABLE ERROR (01)	CORRECTABLE DATA CHECK (18)	**REASSIGN BLOCK, READ, READ (EXTENDED), WRITE, WRITE (EXTENDED), SEEK, SEEK (EXTENDED), COPY, SEND DIAGNOSTIC, RECEIVE DIAGNOSTIC, WRITE AND VERIFY, VERIFY**
NOT READY (02)	DRIVE NOT READY (04)	**TEST UNIT READY, REZERO UNIT, FORMAT UNIT, REASSIGN BLOCK, READ, WRITE, SEEK, COPY, RECEIVE DIAGNOSTIC, SEND DIAGNOSTIC, WRITE AND VERIFY, VERIFY**

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Table A-1. General Error Conditions (continued)

Sense Key	Sense Code	Applicable Command
MEDIUM ERROR (03)	NO SEEK COMPLETE (02) UNCORRECTABLE DATA ERROR (11), BLOCK NOT FOUND (14), SEEK ERROR (15), BAD SECTOR FILE FULL (35), BAD SECTOR FILE INACCESSIBLE (36)	FORMAT UNIT, REASSIGN BLOCK, READ, WRITE, VERIFY, COPY, WRITE AND VERIFY, RECEIVE DIAGNOSTIC, READ (EXTENDED), WRITE (EXTENDED)
HARDWARE ERROR * (04)	Drive-related errors, DATA TRANSFER INCOMPLETE (1B), CONTROLLER PLL ERROR (1E), NO TRACK ZERO (06), WRITE FAULT (03)	TEST UNIT READY, COPY, REZERO UNIT, FORMAT UNIT, REASSIGN BLOCK, READ, WRITE, SEEK, RECEIVE DIAGNOSTIC, SEND DIAGNOSTIC, WRITE AND VERIFY, VERIFY
ILLEGAL REQUEST (05)	INVALID COMMAND (20) ILLEGAL BLOCK ADDRESS (21)	All commands
UNIT ATTENTION (06)	UNIT ATTENTION (30)	All commands
DATA PROTECT (07)	WRITE PROTECTED (17)	All commands
RESERVED (08)		
VENDOR UNIQUE (09)	DRIVE NOT SELECTED (05) COMMAND TIMEOUT (31)	FORMAT UNIT, TEST UNIT READY

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Table A-1. General Error Conditions (continued)

Sense Key	Sense Code	Applicable Command
COPY ABORTED ** (0A)	---	COPY
ABORT COMMAND (0B)	---	All commands
EQUAL (0C) **	---	SEARCH DATA EQUAL, SEARCH DATA LOW, SEARCH DATA HIGH
VOLUME OVERFLOW (0D)	---	No commands
MISCOMPARE (0E)	BAD BLOCK FOUND (19)	VERIFY, WRITE AND VERIFY

* The MD01 Controller does not return a Logical Block Address in the Sense data for this Sense key.

** The MD01 Controller does not return Sense keys and Sense class and codes for non-Standard Sense bytes.